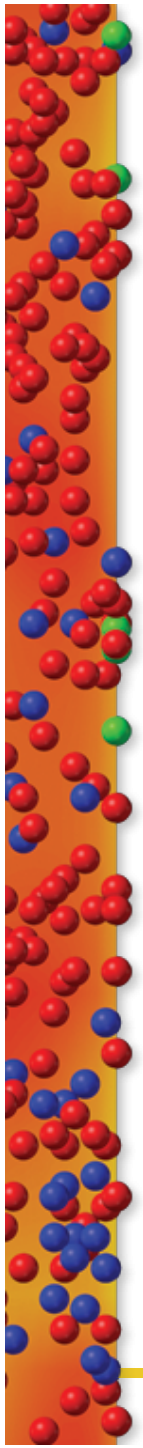
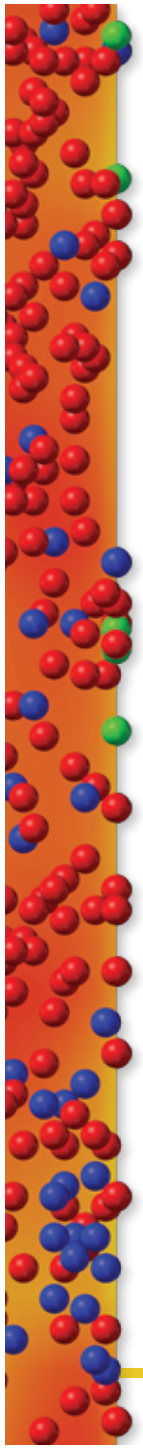


Design/Technology Co-Optimisation (DTCO) in the Presence of Acute Variability

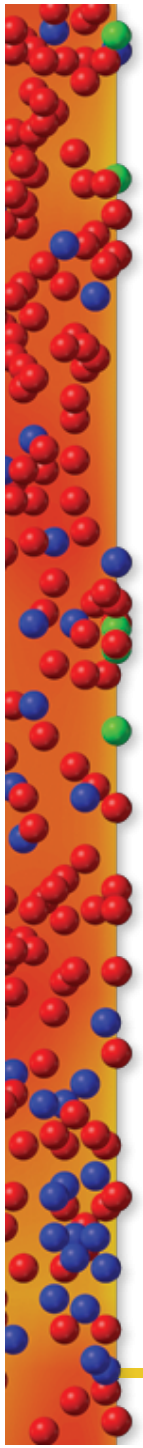
A. Asenov[1,2], E. A. Towie[1]

[1]Gold Standard Simulations Ltd
[2]Glasgow University



Summary

- Introduction
- FinFET complexity Motivates DTCO
- DTCO flow at 14nm FinFETs
- 10nm FinFETs: *Si vs. Ge*
- Conclusions



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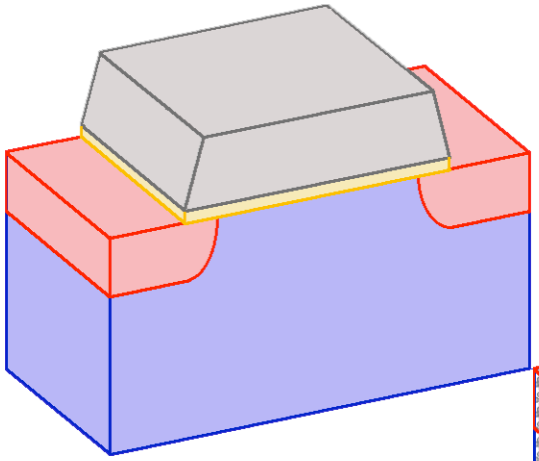
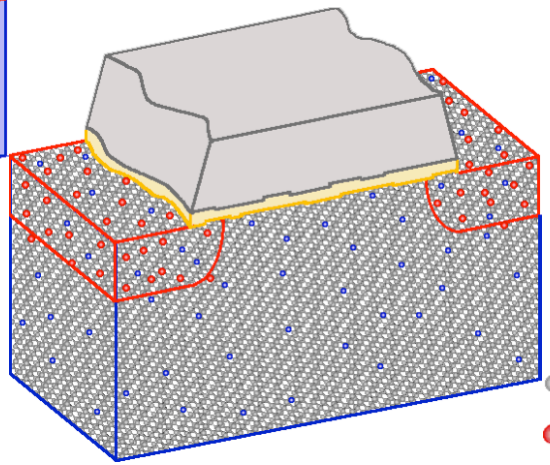
- Conclusions

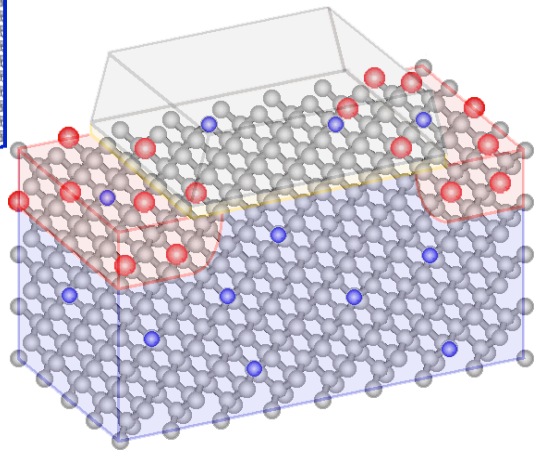
The semiconductor industry is facing atomic scale limitations



The simulation
Paradigm now



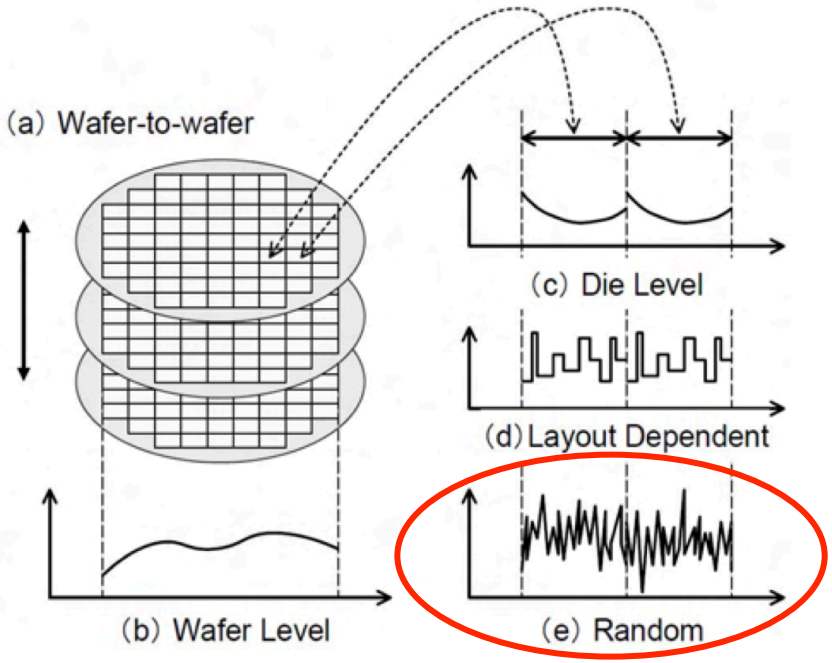
A 22 nm MOSFET
In production 2013

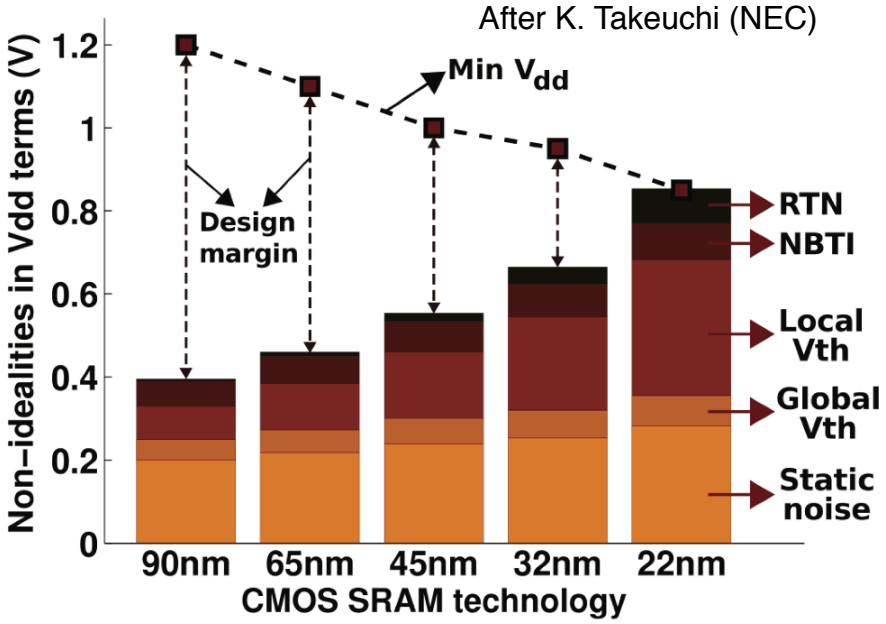


A 4.2 nm MOSFET
In production ????

A. Asenov 1998

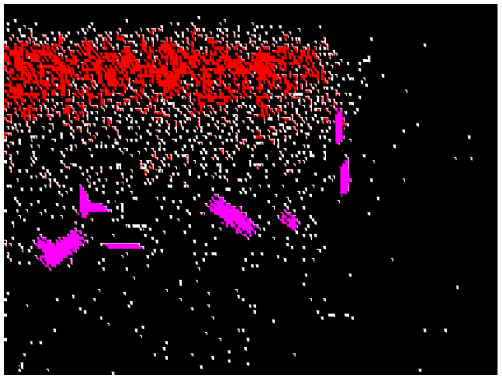
Statistical variability is one of the major challenges associated with scaling

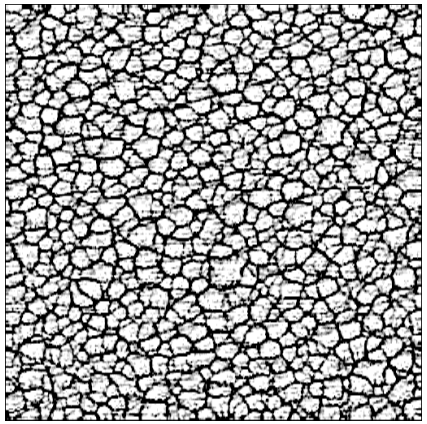


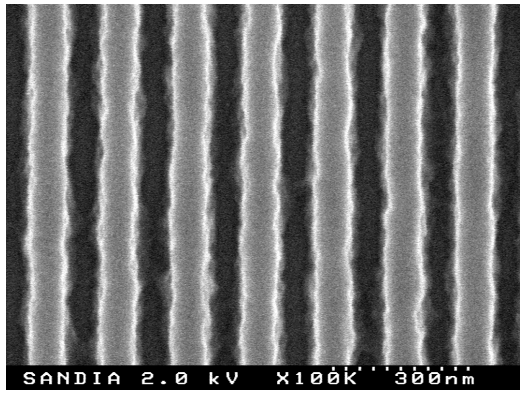


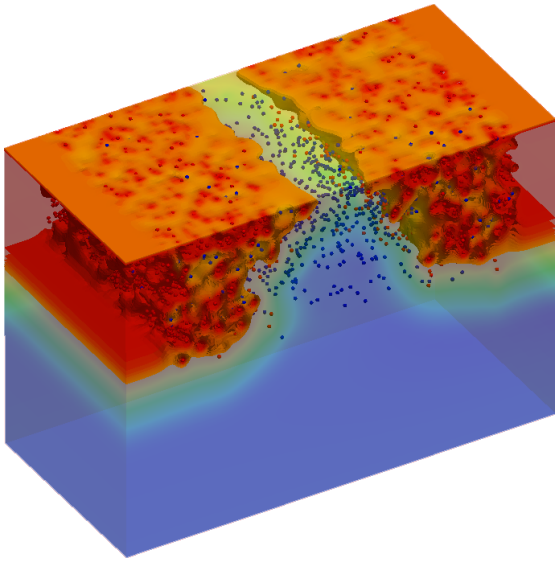
Variability results in higher parametric yield loss

Main sources of statistical variability

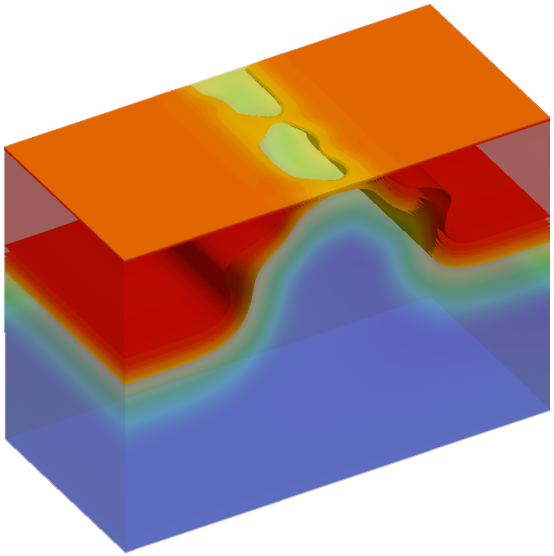




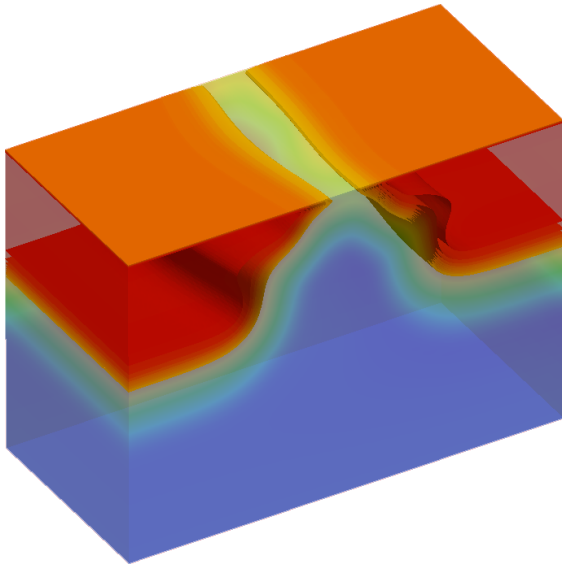




Random dopants

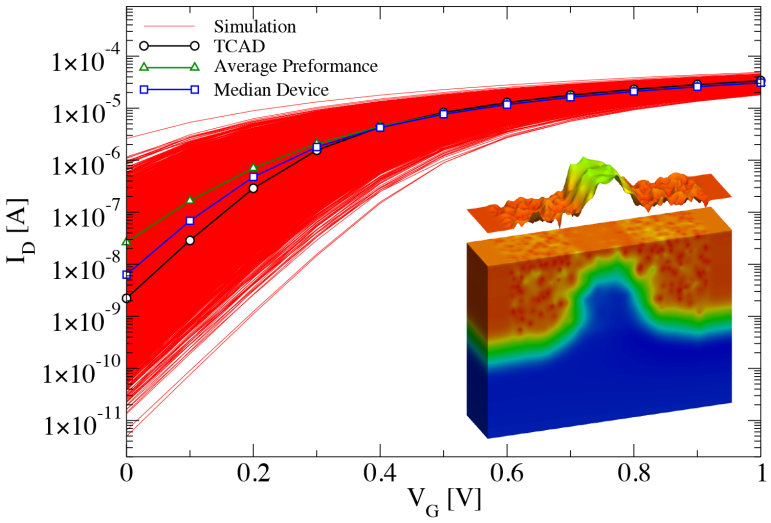


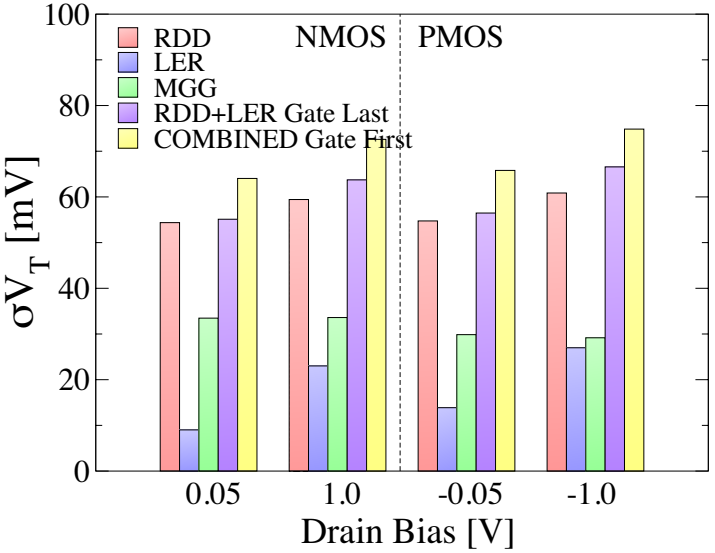
Metal Gate Granularity

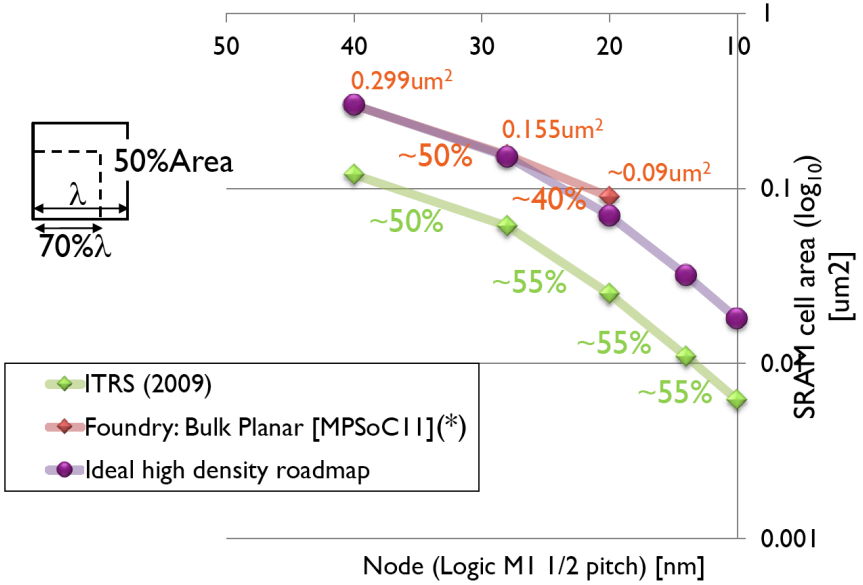


Line edge roughness

Statistical variability in 20nm CMOS



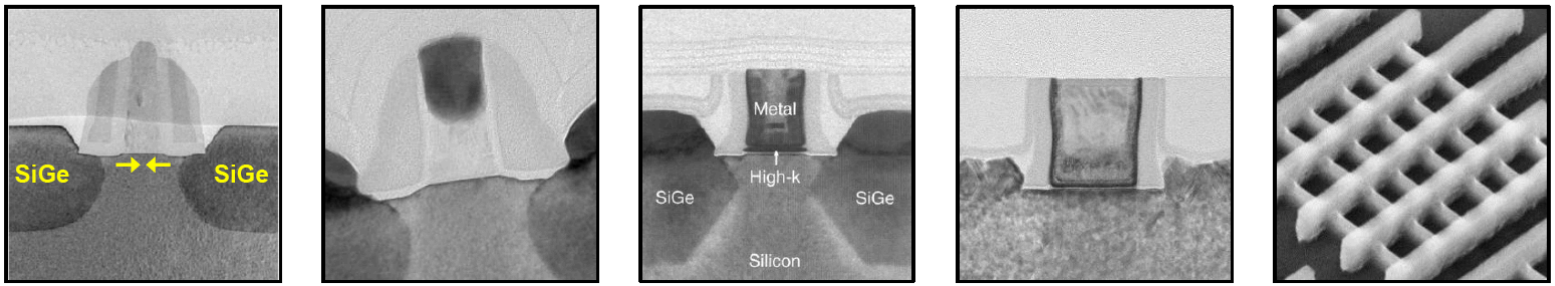




P. Zuber, IMEC

Saturation in performance and increasing variability drives the CMOS innovations

2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm



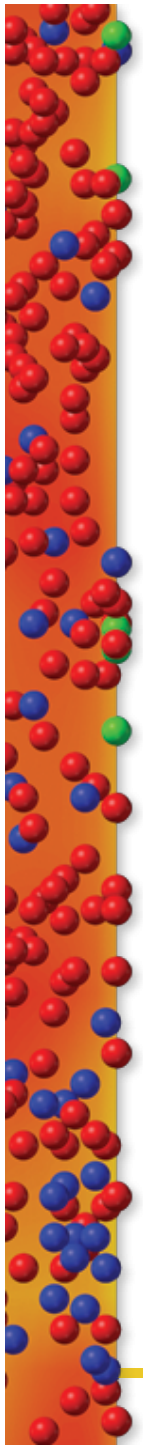
Invented SiGe Strained Silicon M Bohr (Intel)	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

Strained Silicon

High-k Metal Gate

Tri-Gate

FinFETs improve performance and can reduce statistical variability



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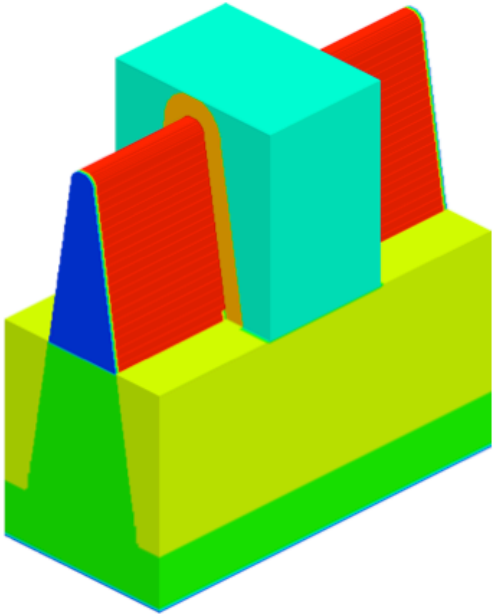
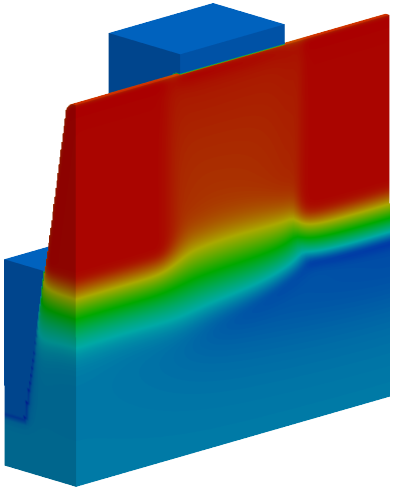
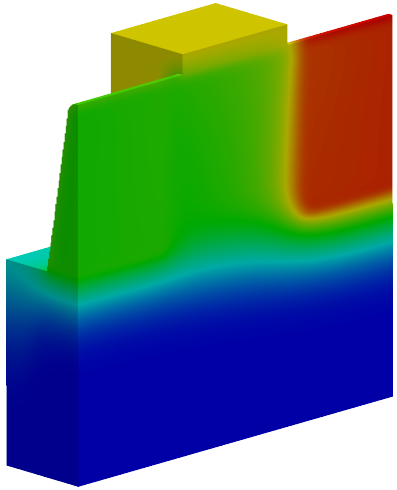
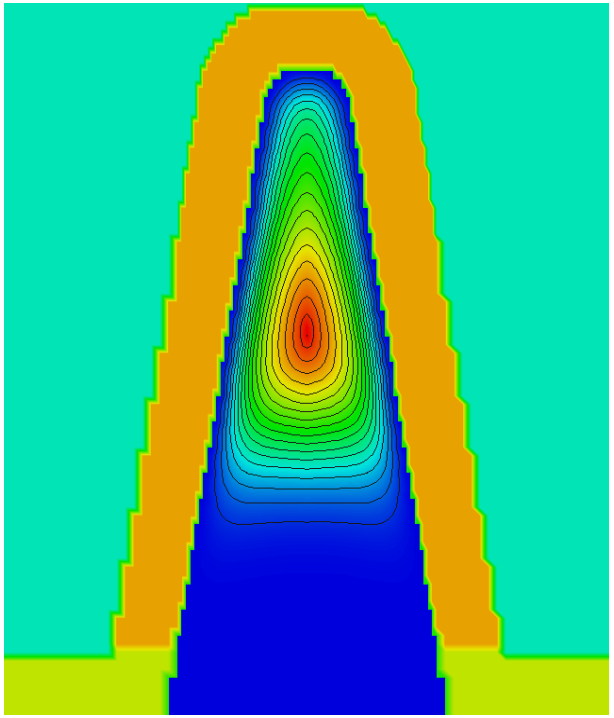
Intel 22nm FinFETs









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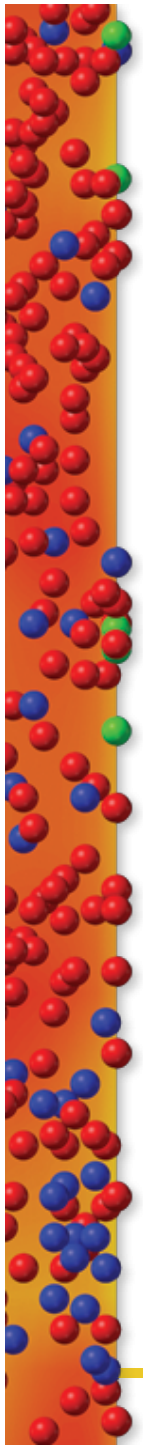
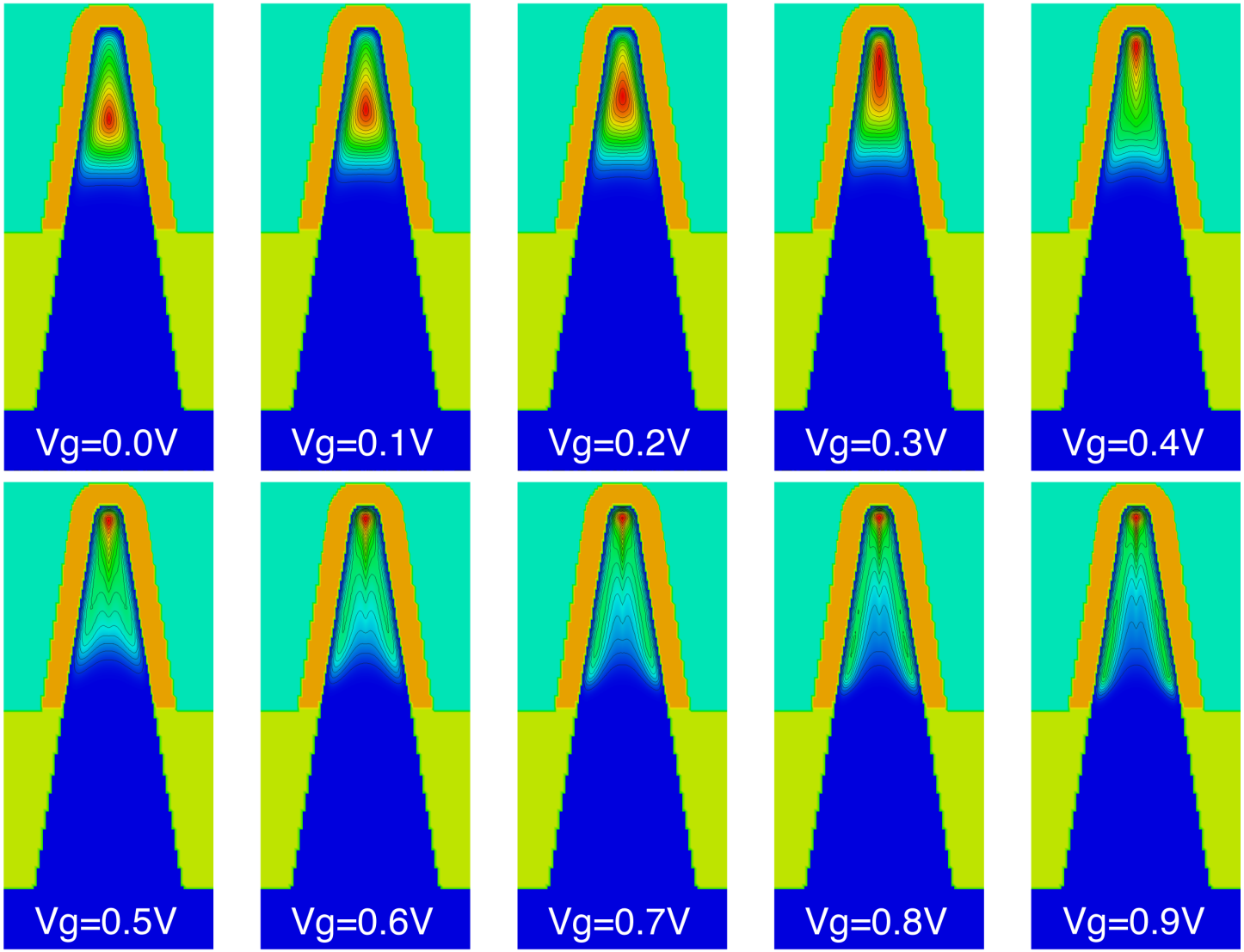
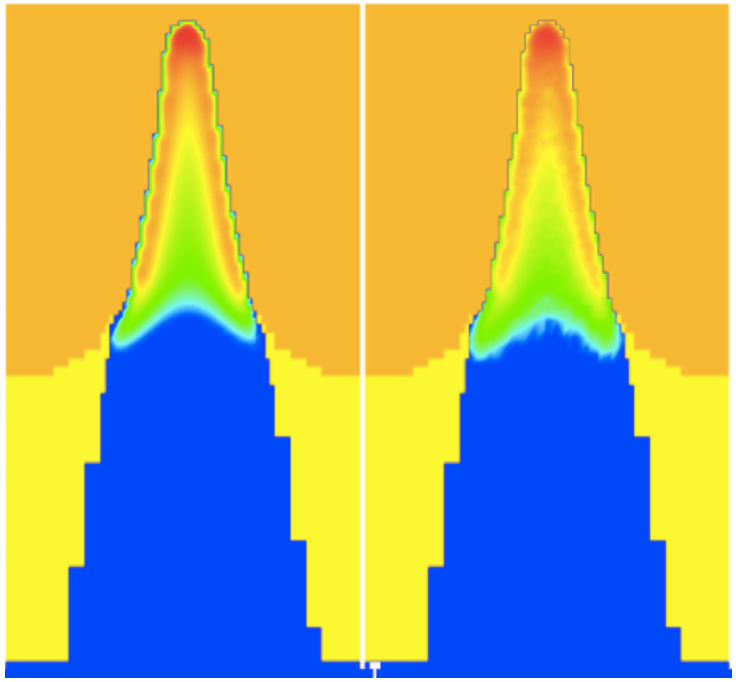




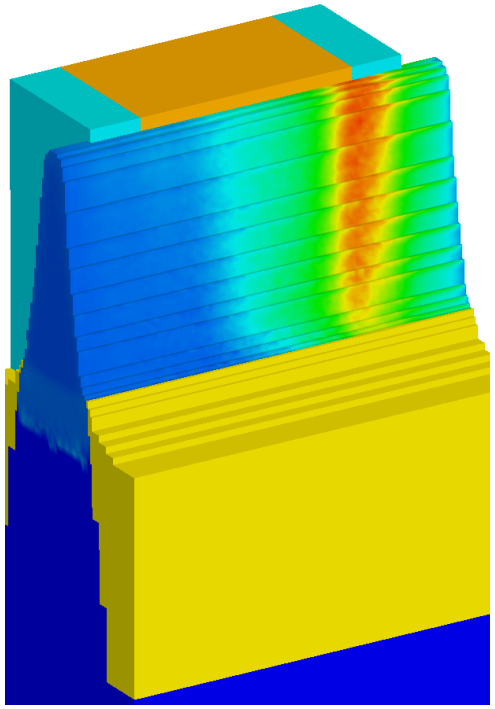
3D Ensemble MC simulation provide predictability

Quantum confinement is important

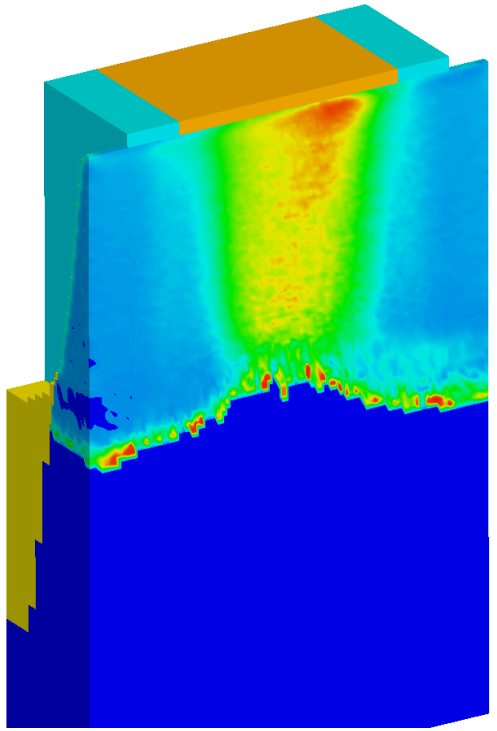
Non-equilibrium transport is also important



DD MC

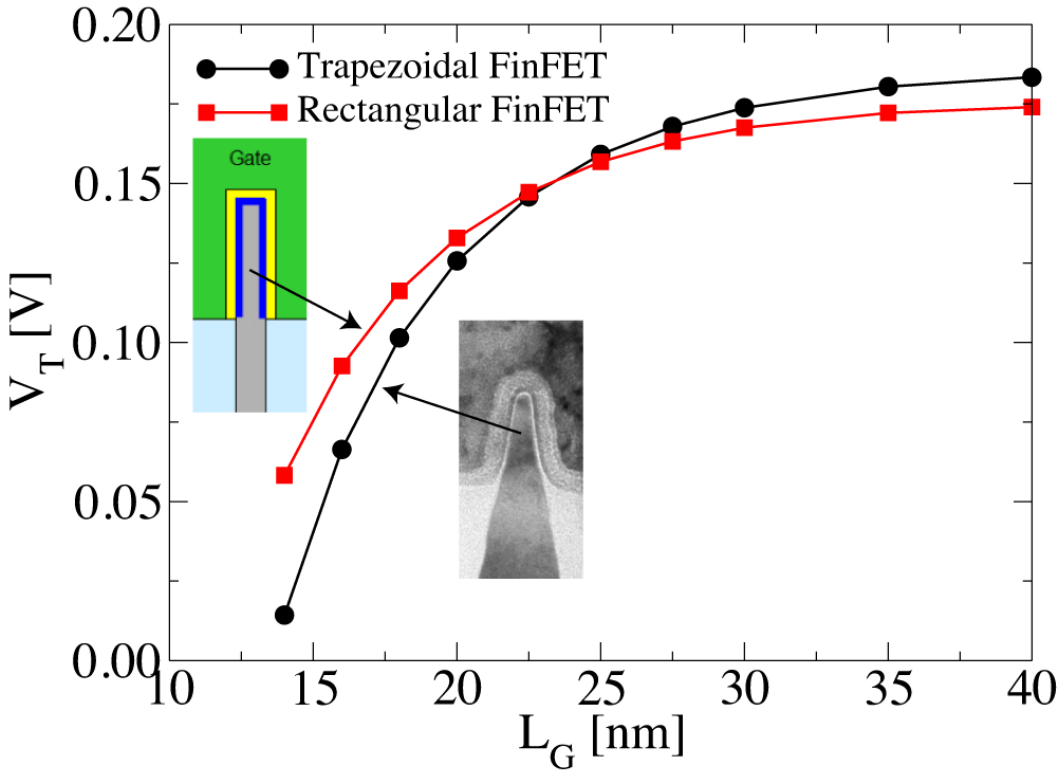


Electron energy

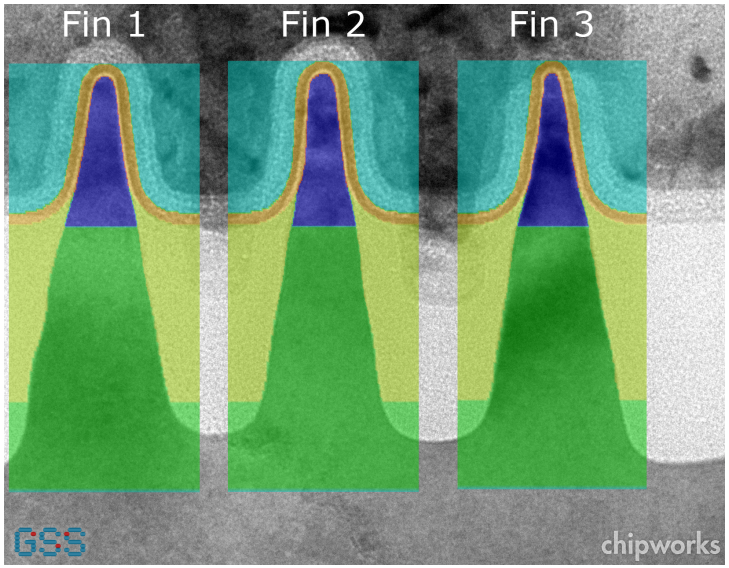


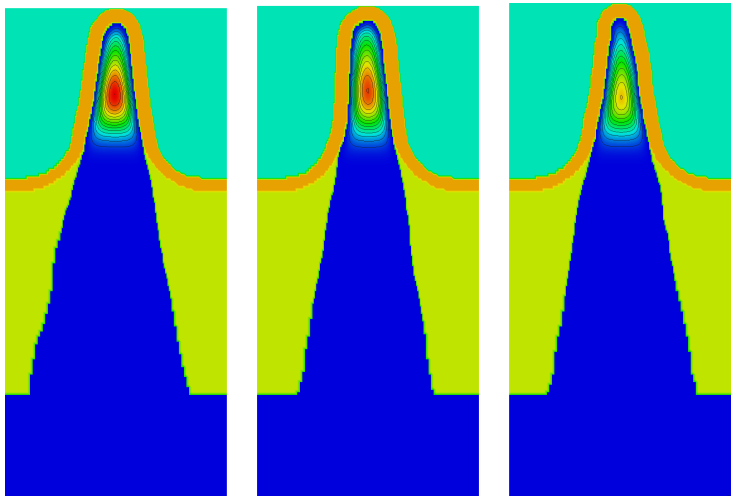
Electron velocity

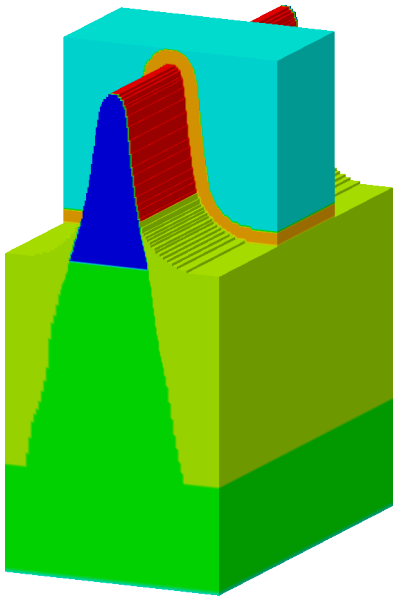
Intel 22nm FinFETs

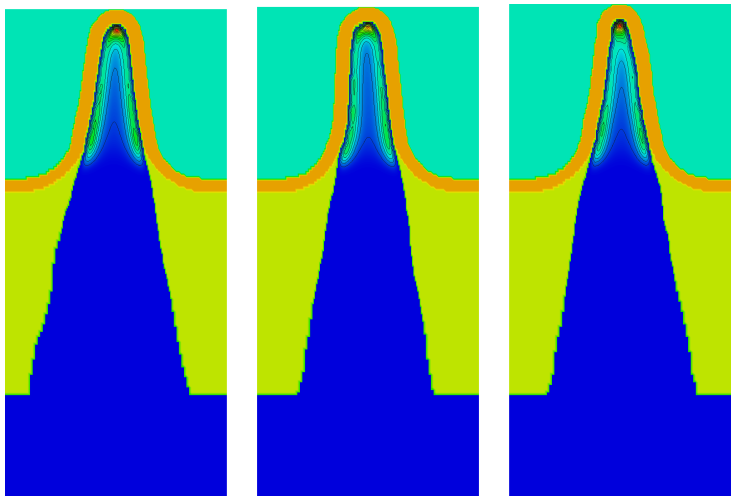


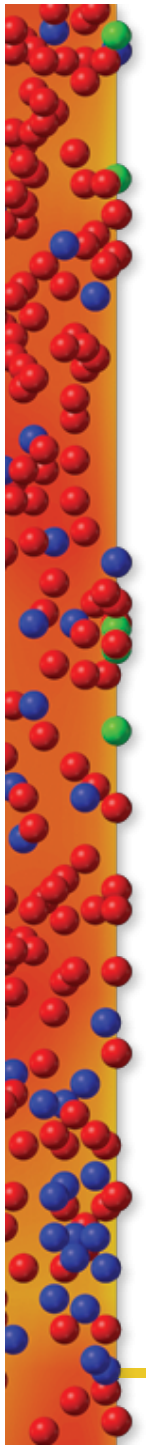
Intel 22nm FinFETs











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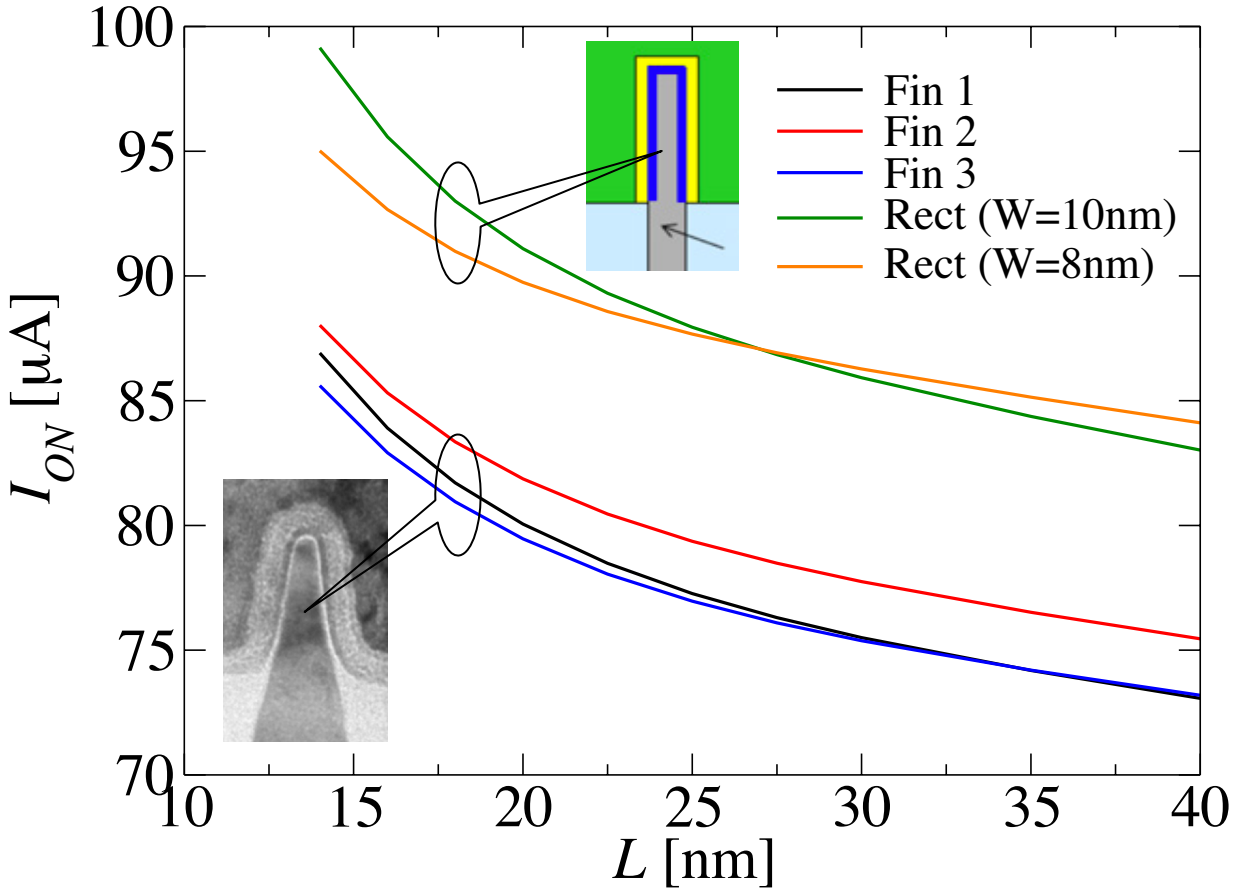
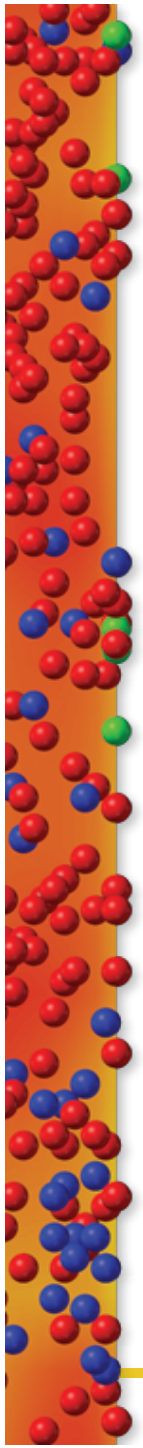


Rectangular fins have 15% higher performance for equivalent width and height.



Summary

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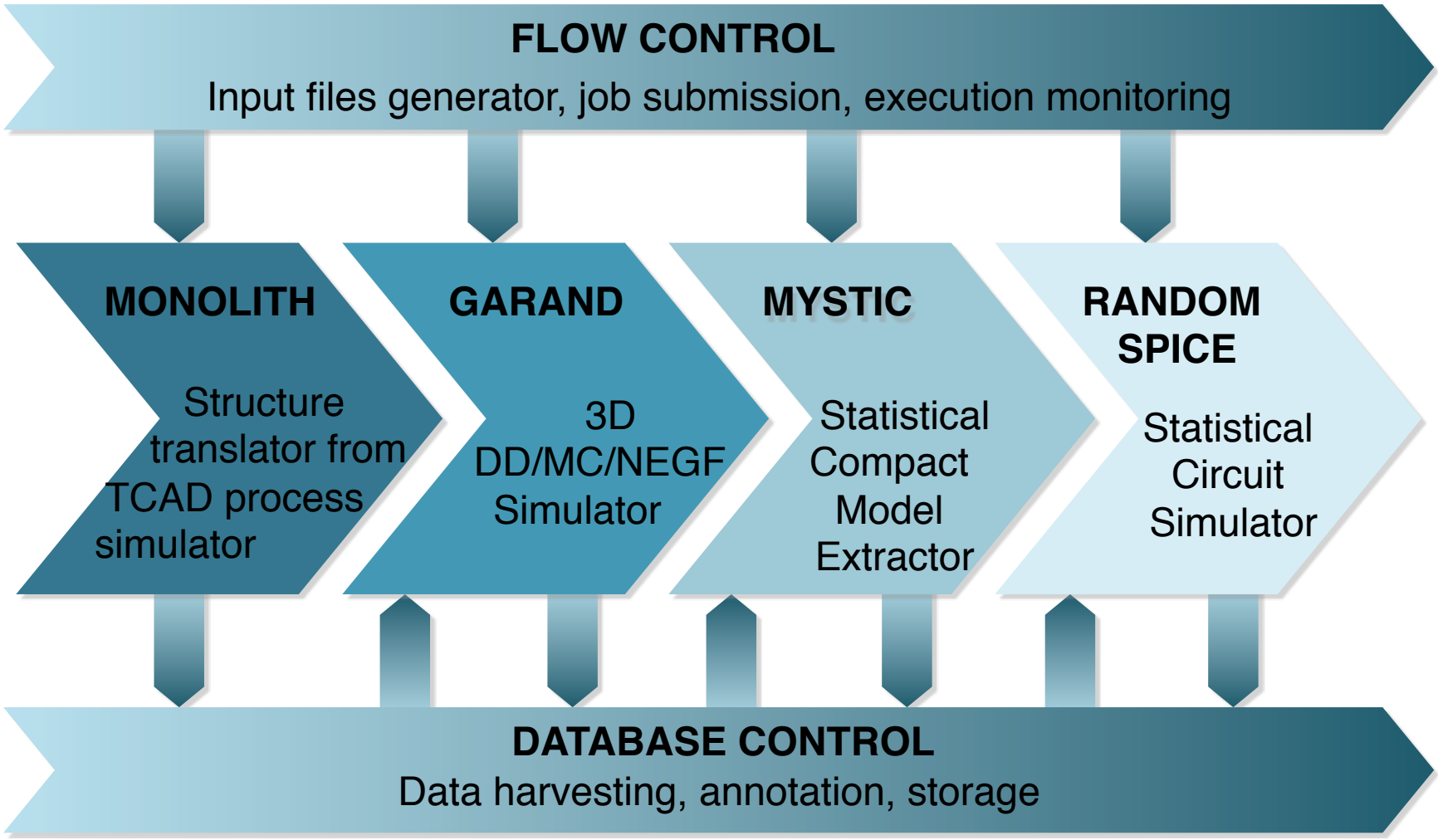
- FinFET complexity Motivates DTCO
- DTCO flow at 14nm FinFETs
  - Predictive TCAD simulation
  - Statistical CM extraction
  - Statistical Circuit simulation
- 10nm FinFETs: *Si vs. Ge*
- Conclusions

The GSS Tool Suite that enables the Design Technology Co-Optimization flow



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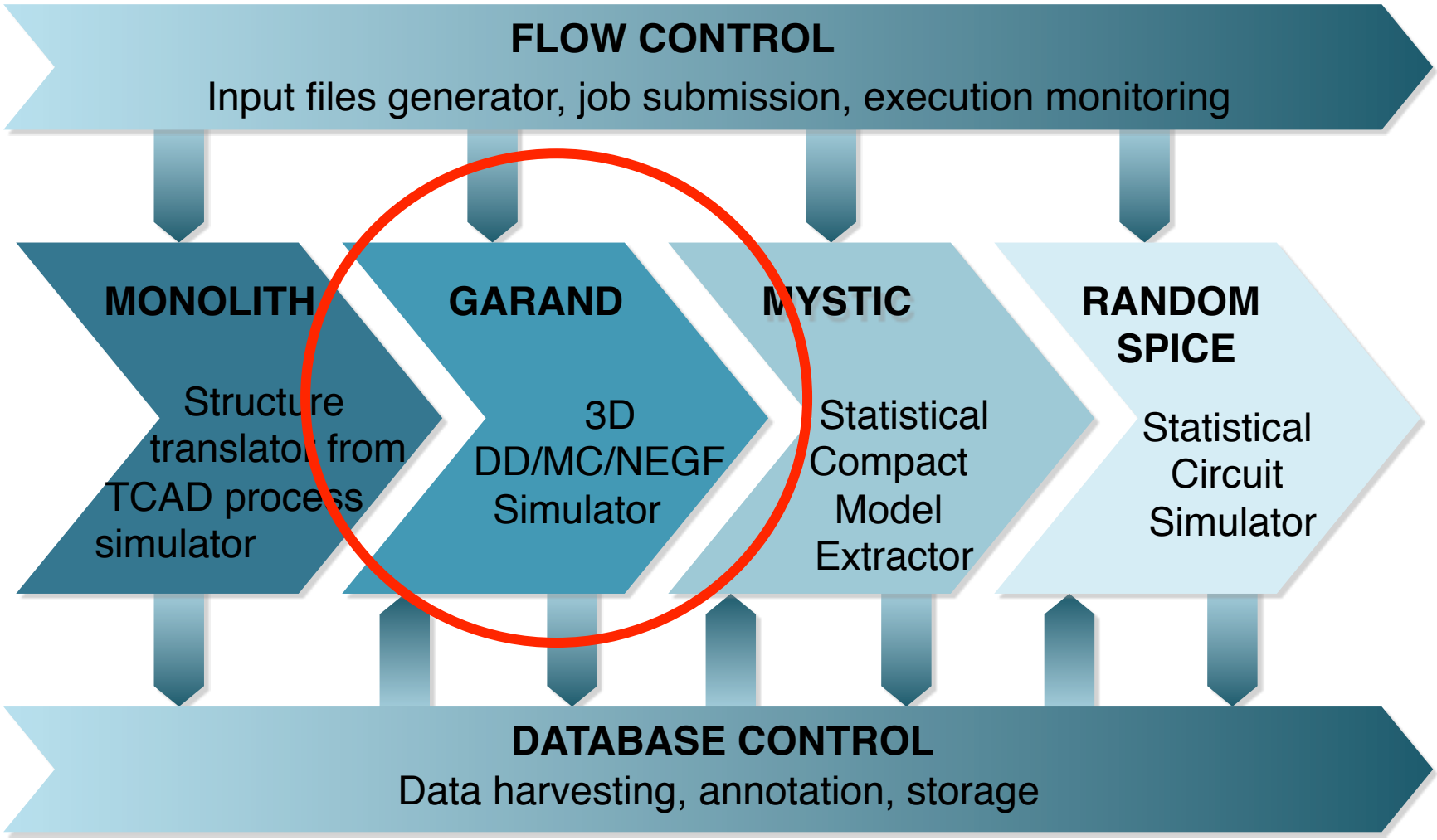
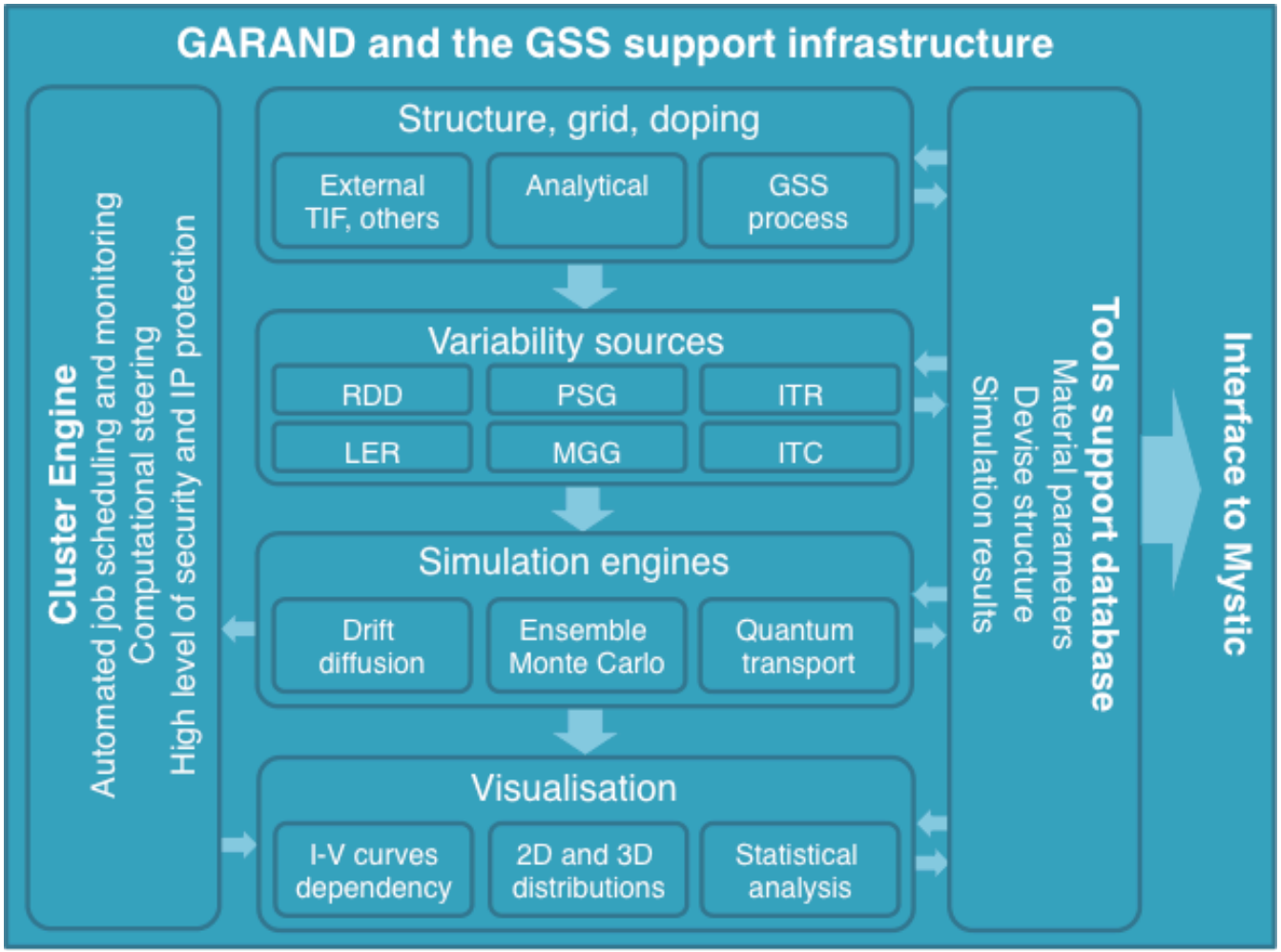
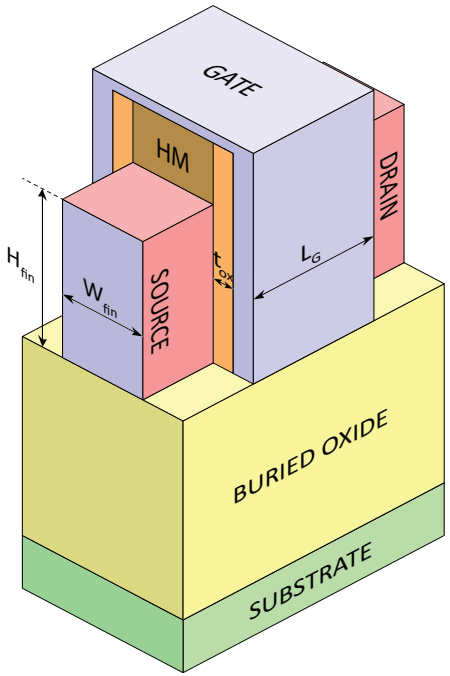


The statistical device simulator GARAND



14nm DG FinFET specification

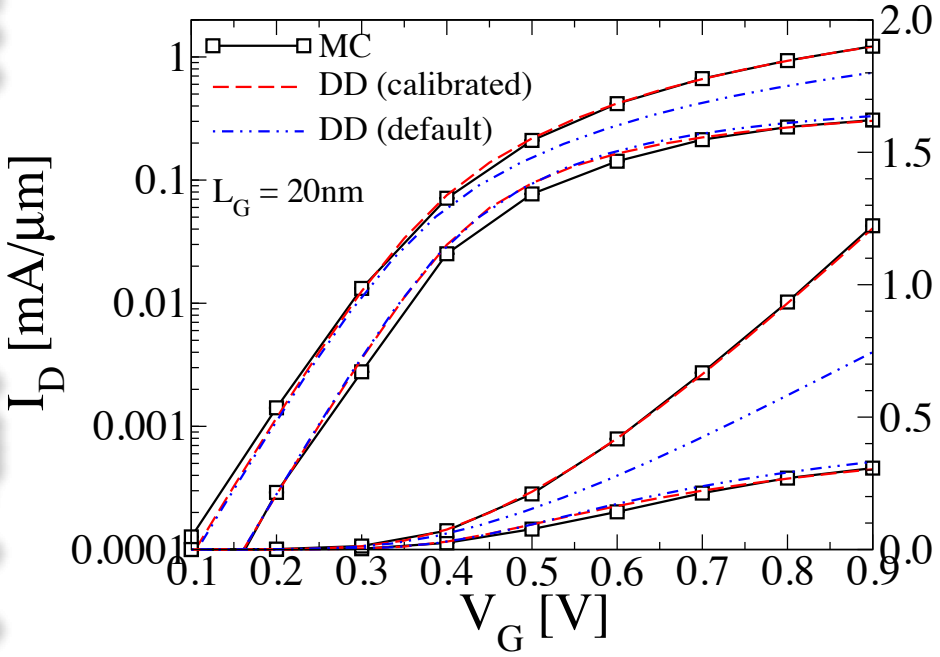


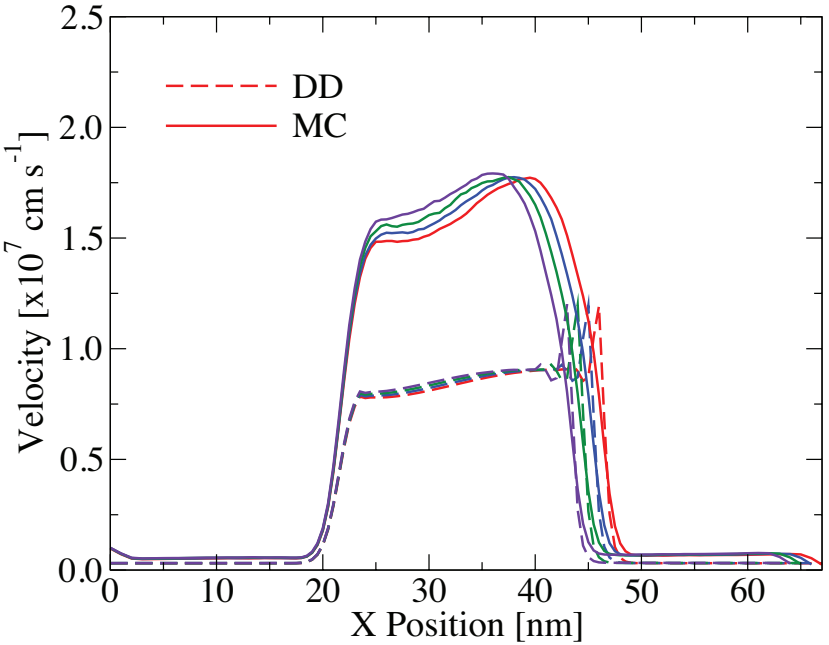
Dimension	Min (nm)	Max (nm)
Fin Width	8	12
Fin Height	22	28
Gate Length	18	22

- Double gate FinFETs targeted at 14nm technology node.
- Devices targeted for high performance SRAM application.
- Process variation aware design.

T=85°C V_{DD} = 0.9V	NMOS	PMOS
I_{ON} (mA/μm)	0.9	0.8
I_{OFF} (nA/μm)	10	10
DIBL(mV/V)	56	65
SS(mV/Dec)	86	88

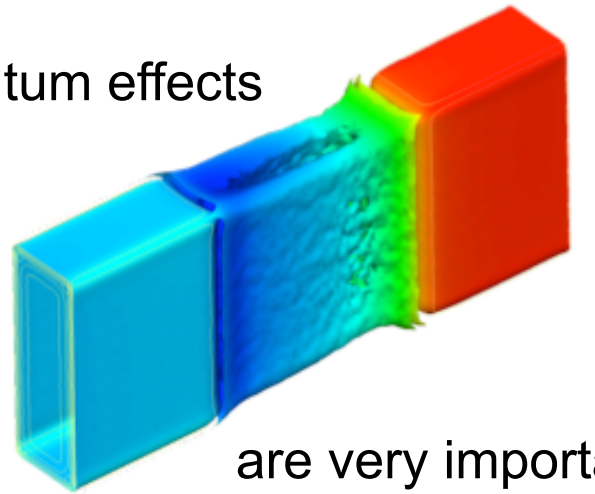
The role of predictive MC simulations





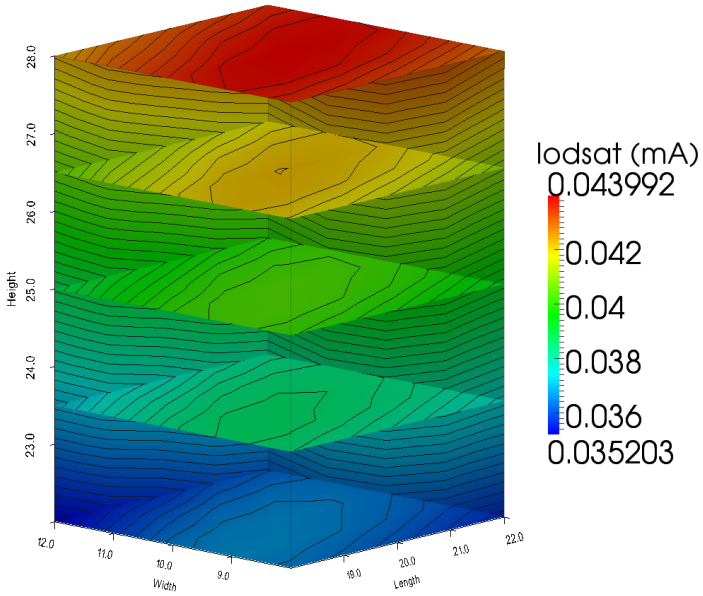
- Only EMC simulations can predict performance.
- Quantum corrections are essential.
- DD simulations can be calibrated to EMC.

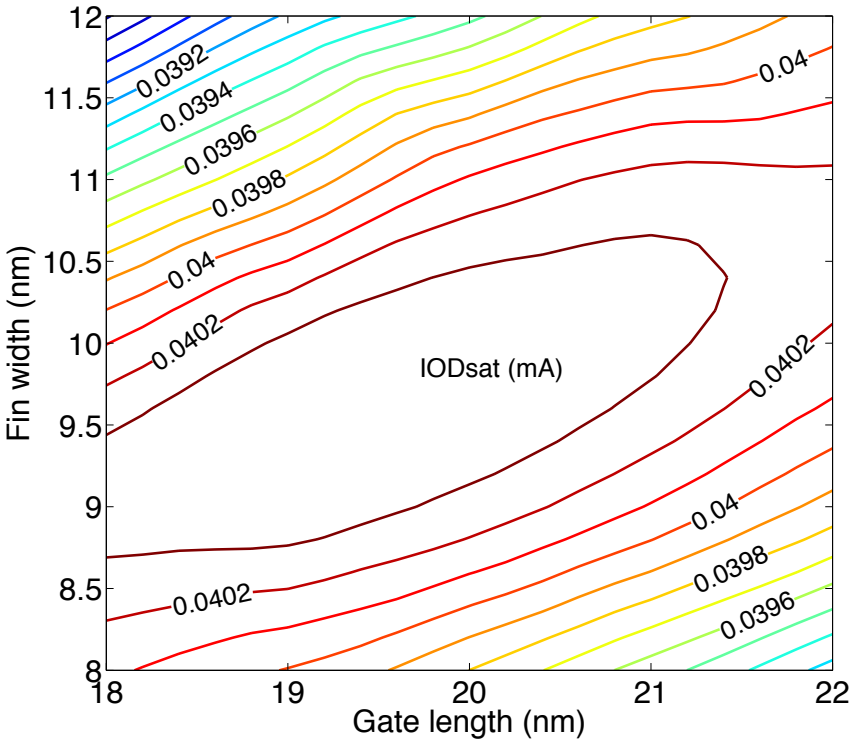
Quantum effects



are very important

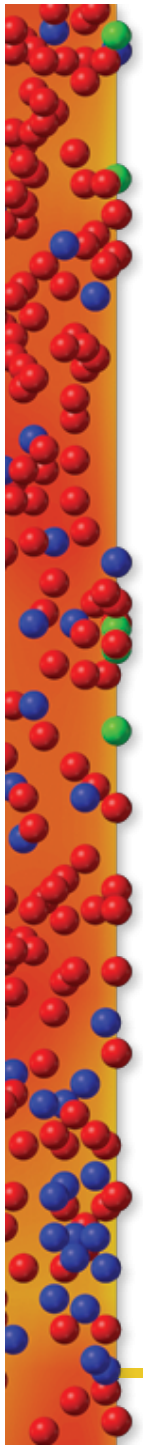
Process induced variability

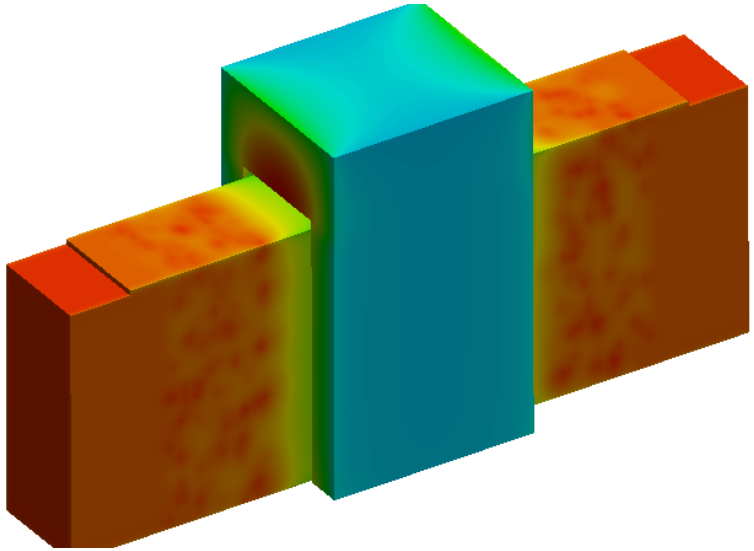


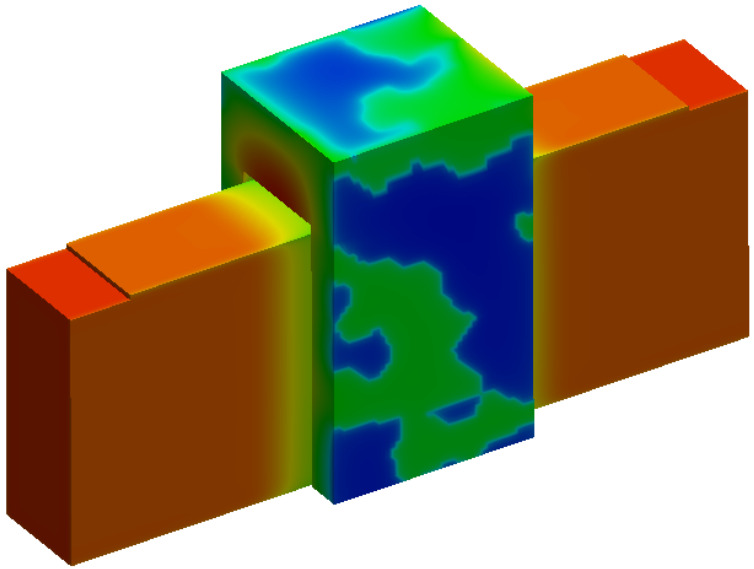


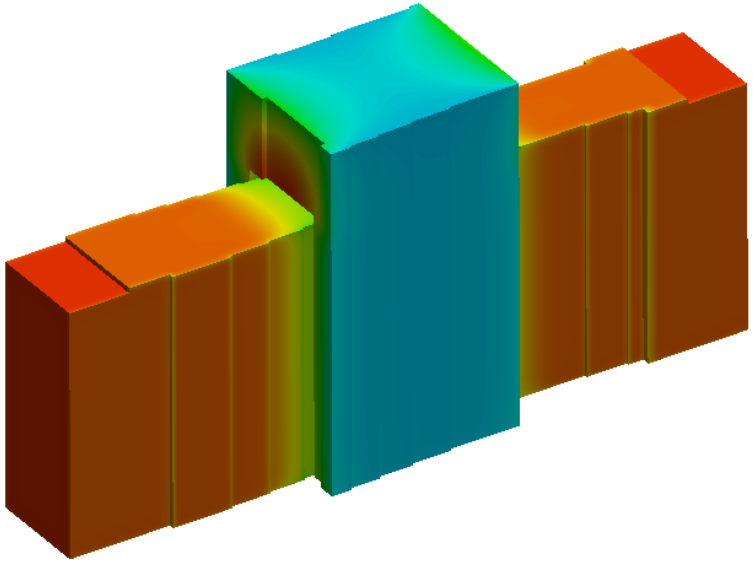
- Captured by experiment design.
- Dependence on L, H_F, W_F, T_{OX}.

Statistical Variability Simulations

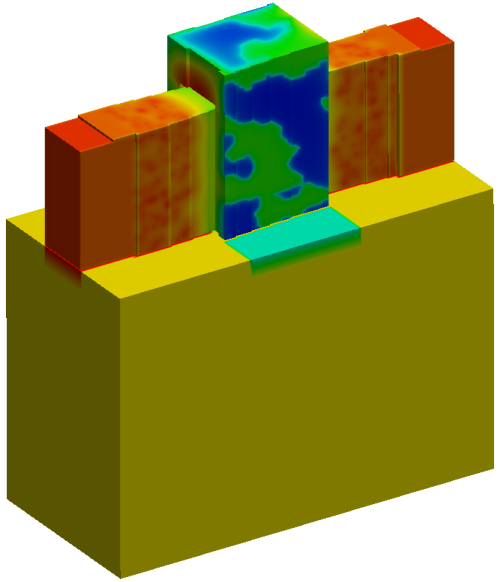


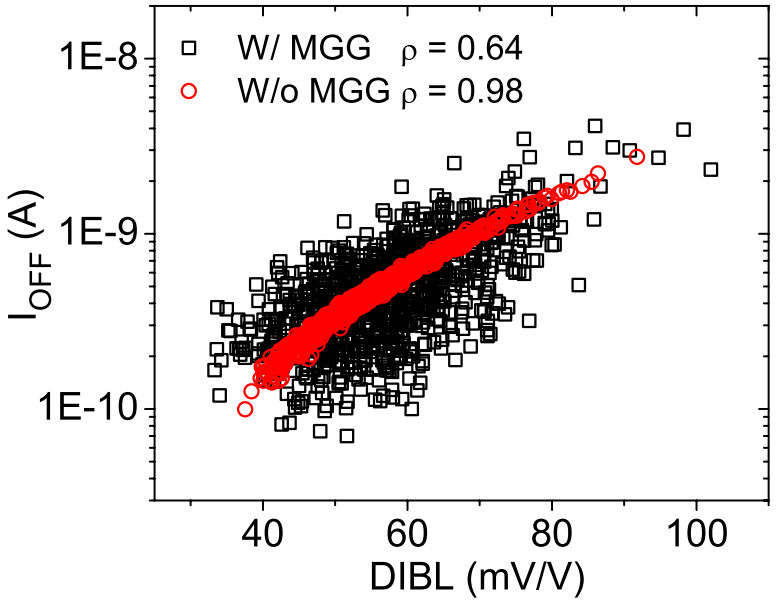


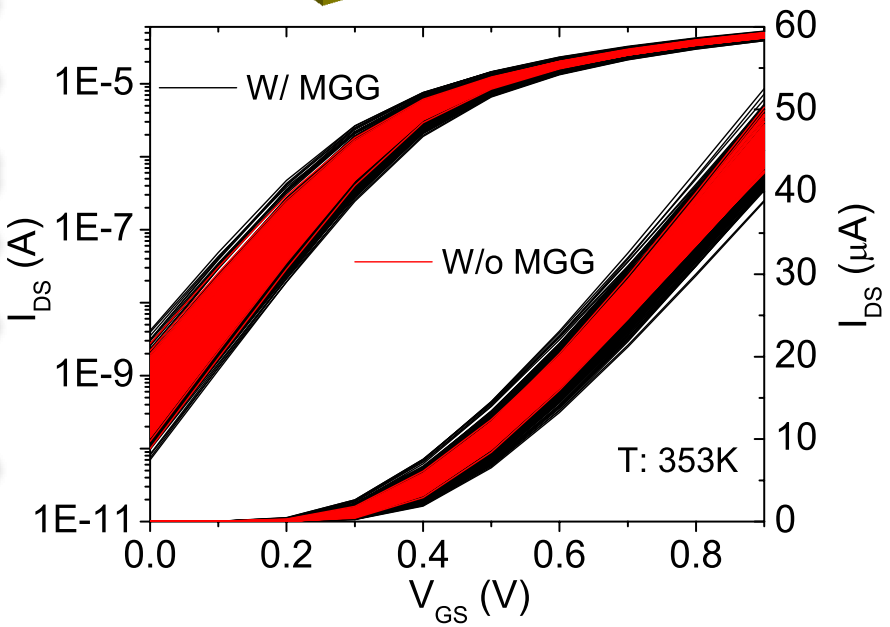




Nominal Device Statistical Variability

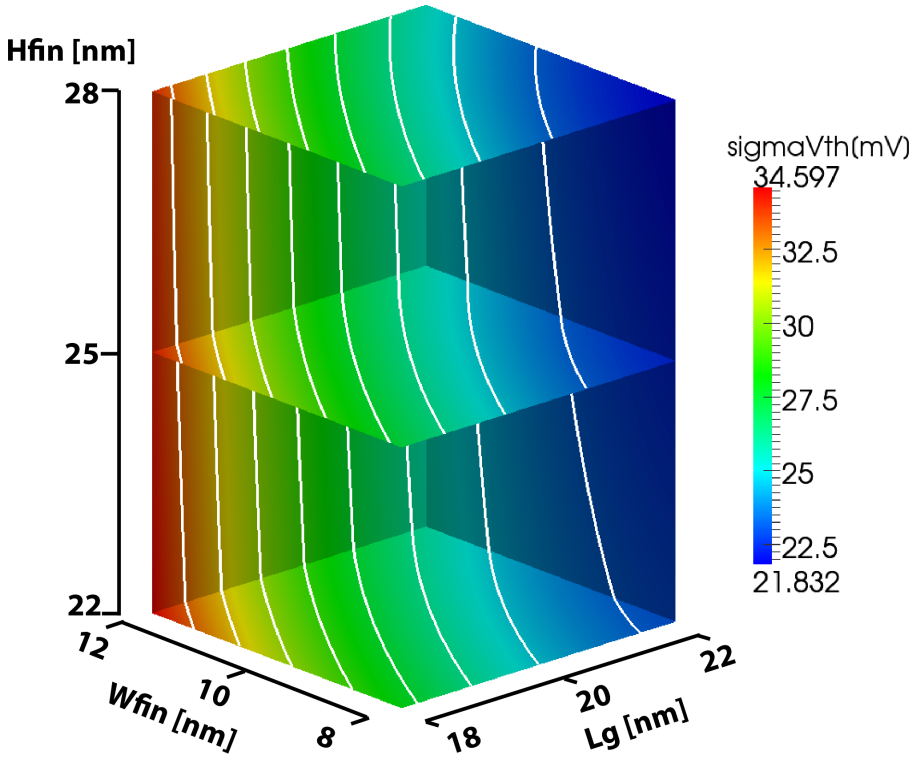


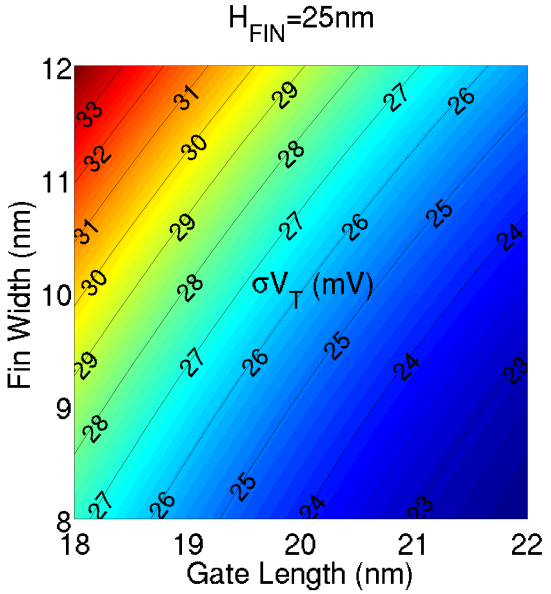


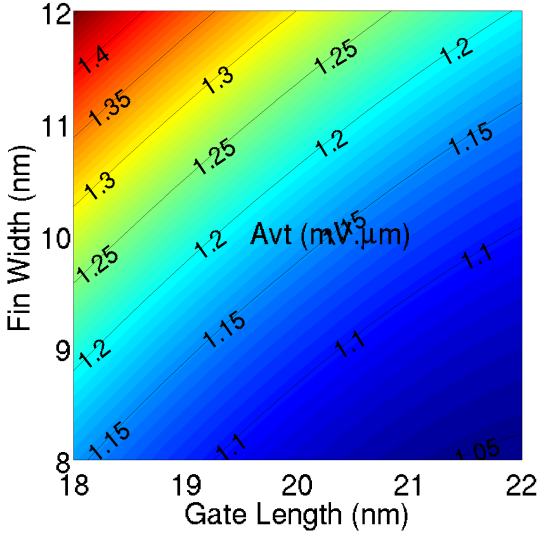


Correlation between subthreshold figure of merits, such as I_{OFF} and DIBL, can be a good indicator to show whether MGG is an active variability source.

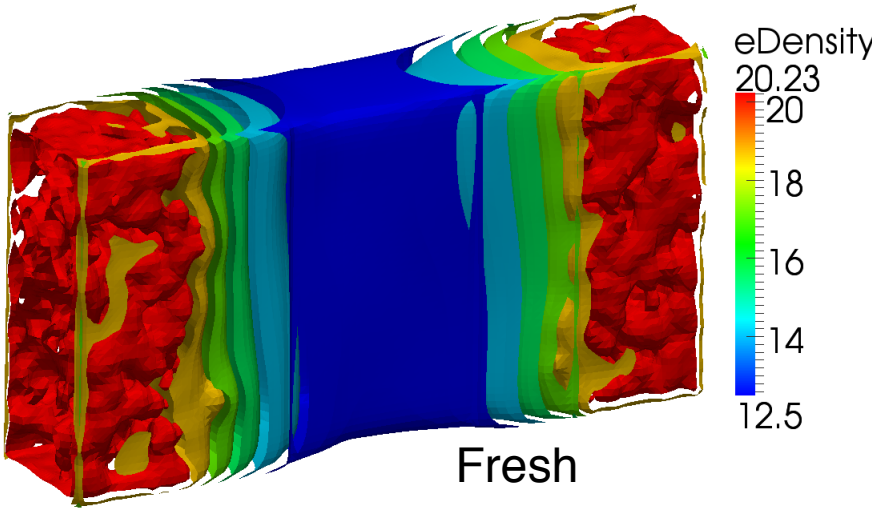
Correlation between process and statistical variability

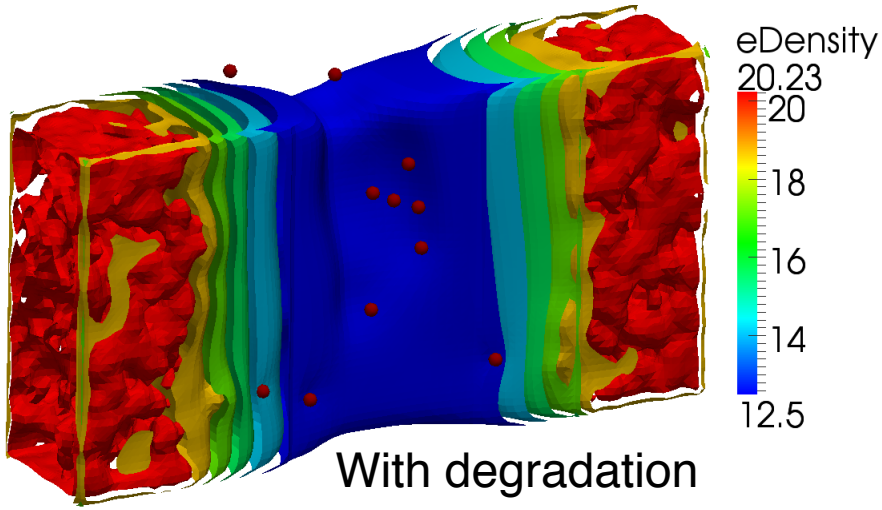


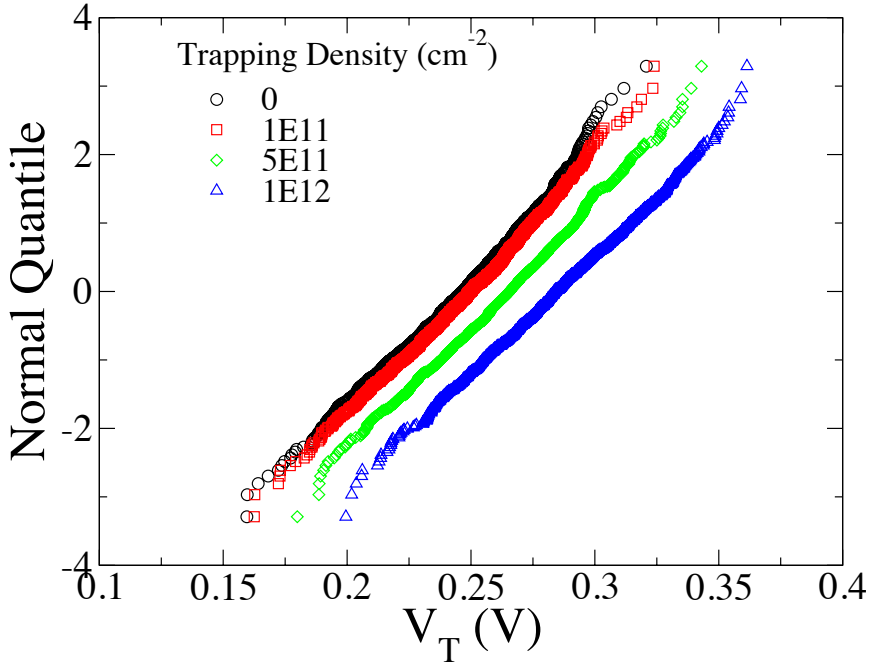


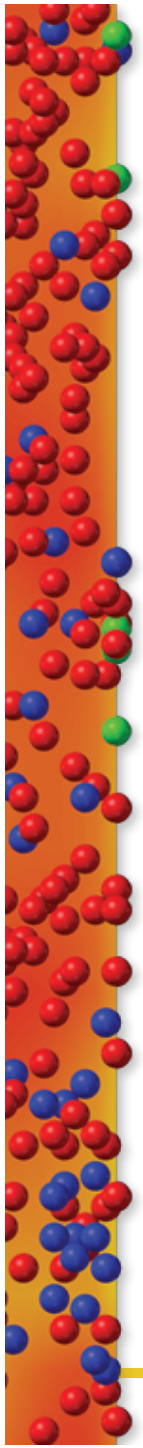


Statistical aspects of Reliability









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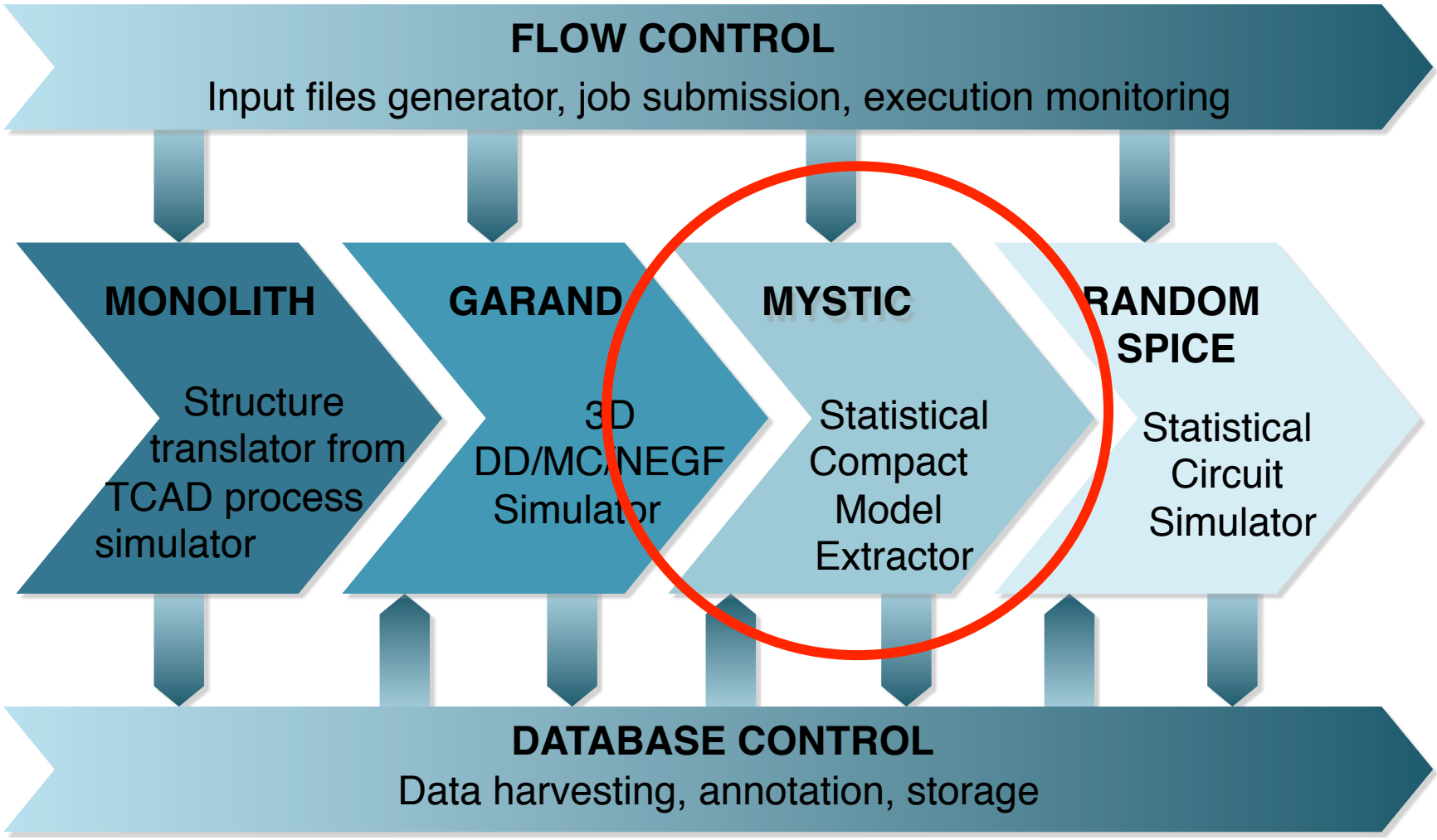
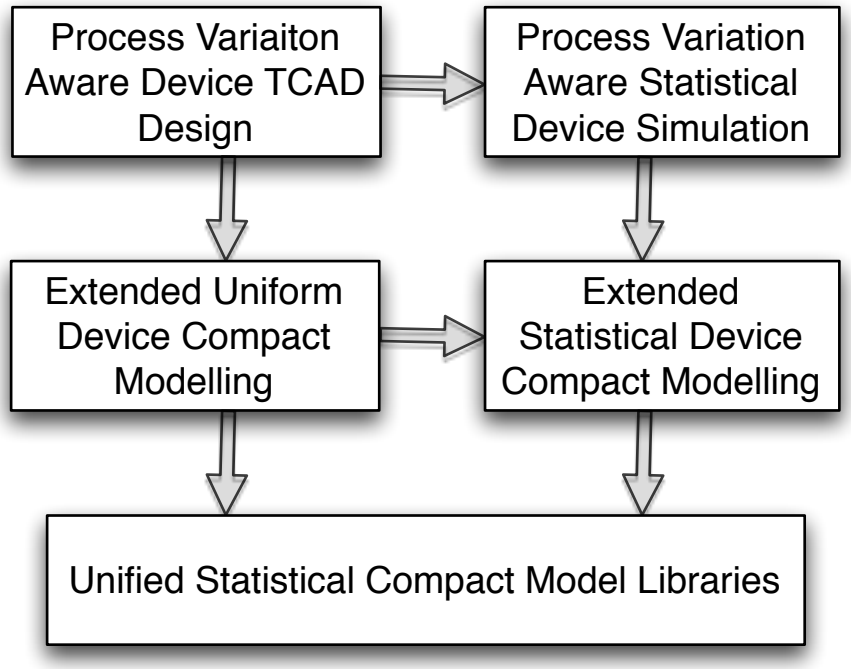
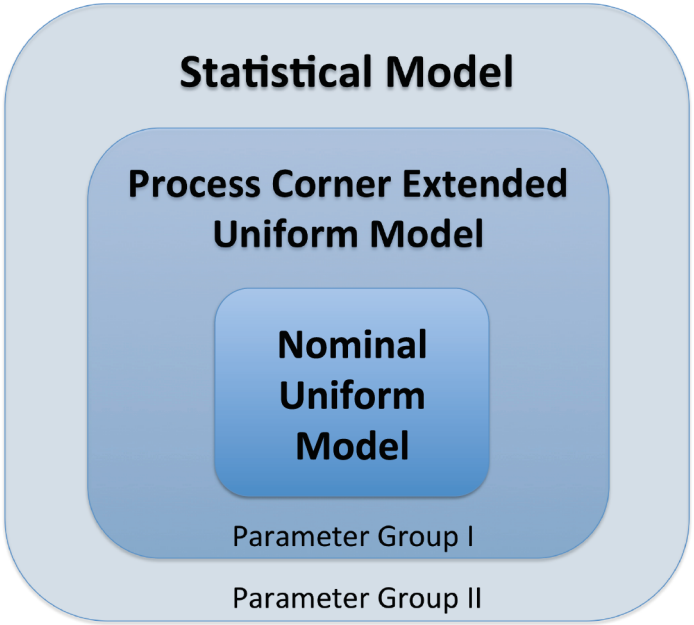
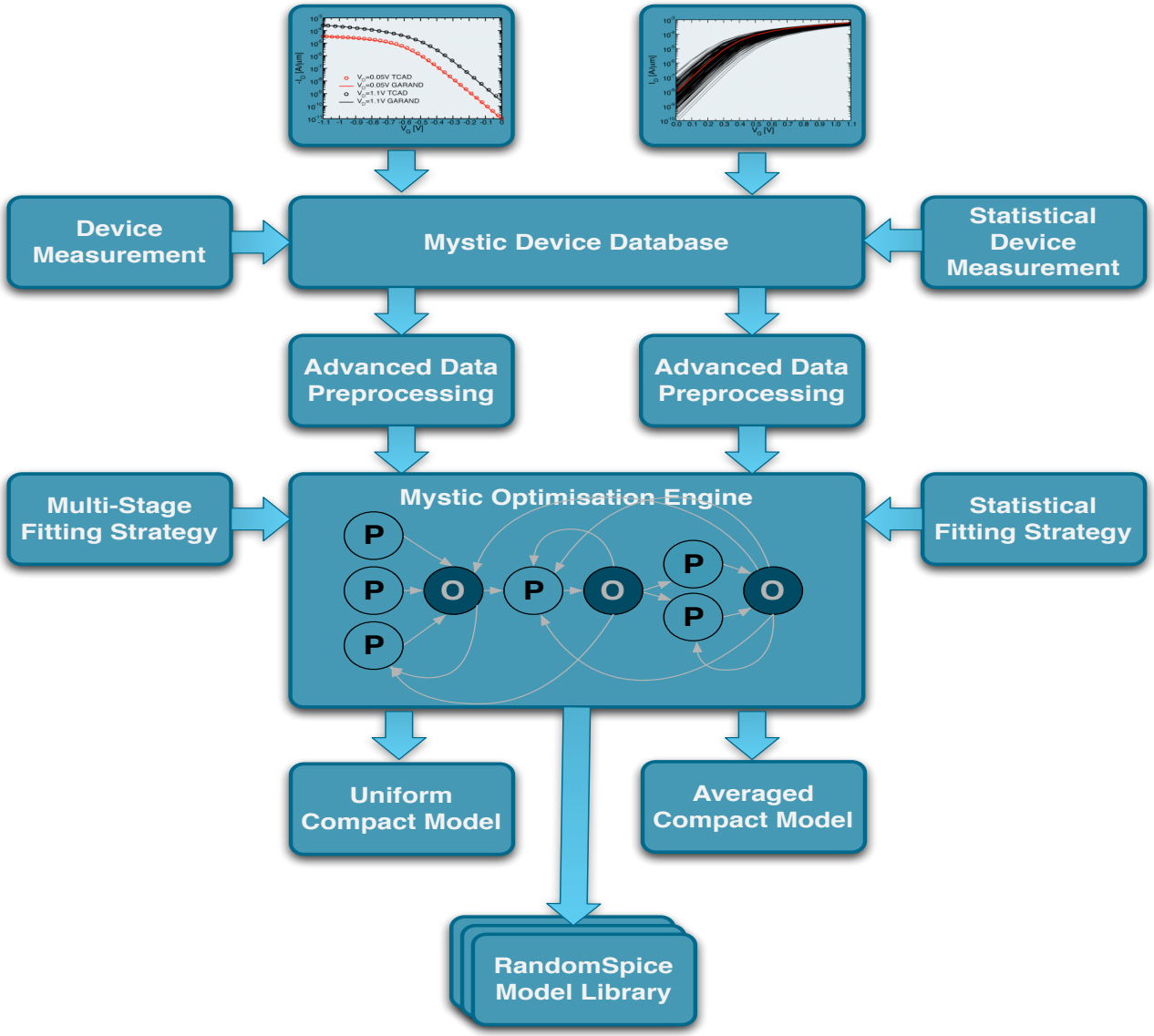


Statistical Compact Modeling Procedure

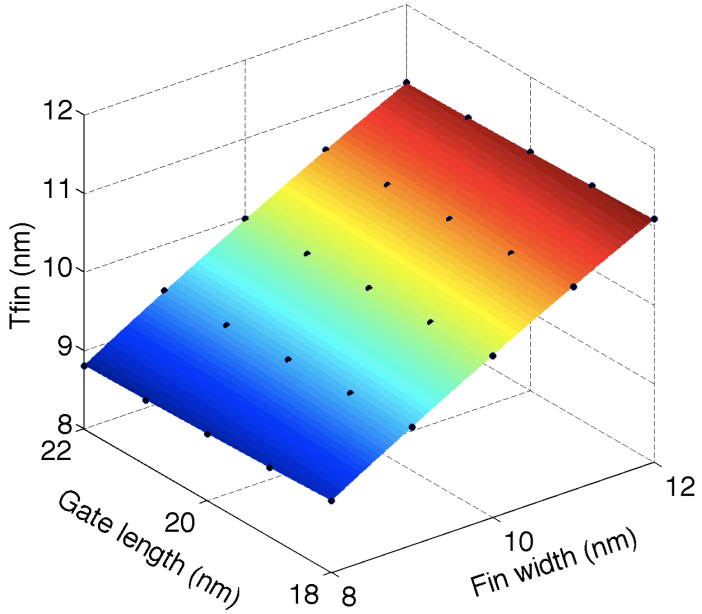


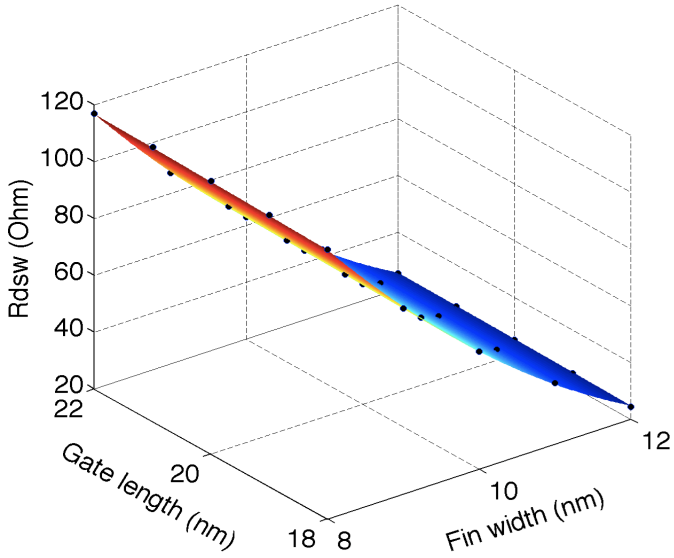


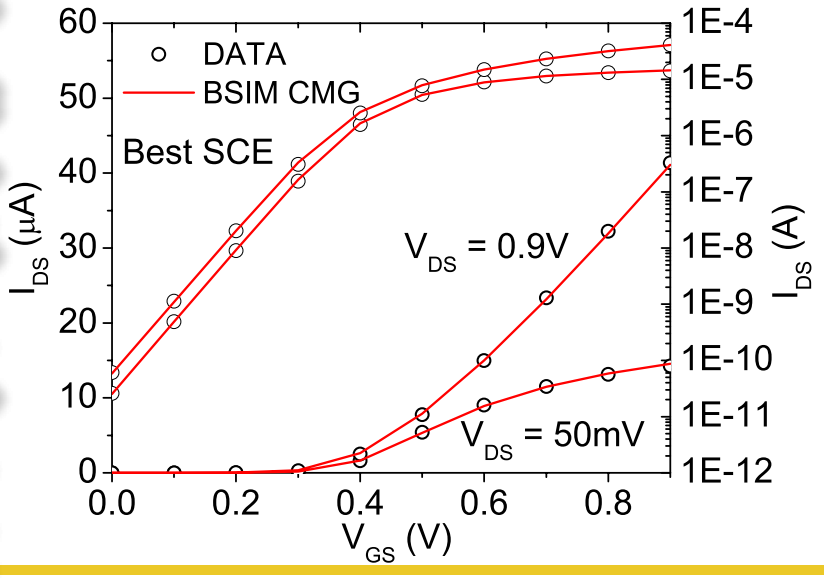
The Statistical Compact Model Extractor Mystic

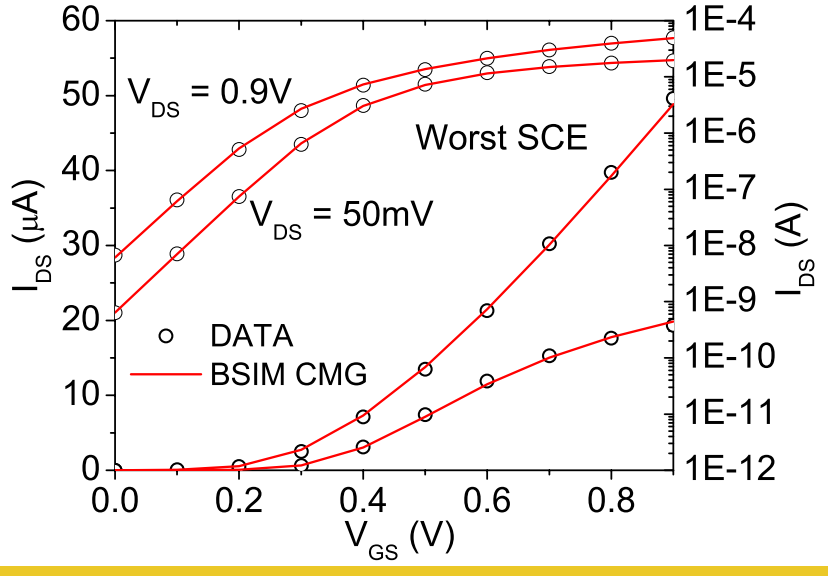


Extended Uniform Model – Group 1 Parameter

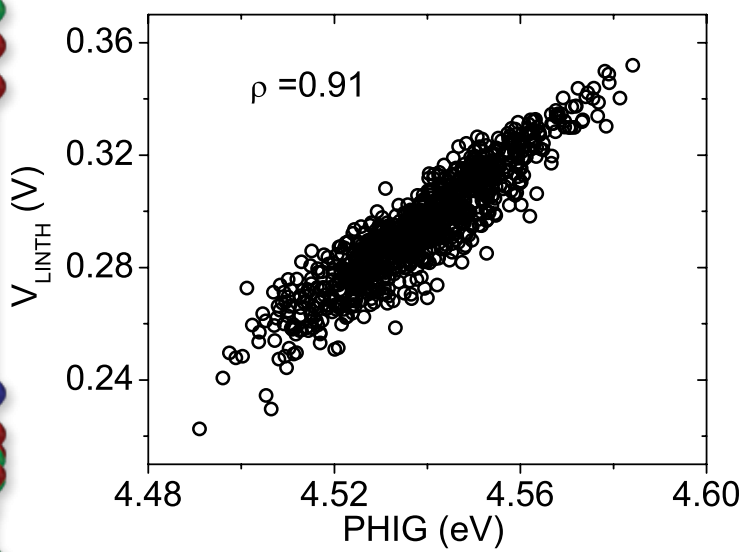


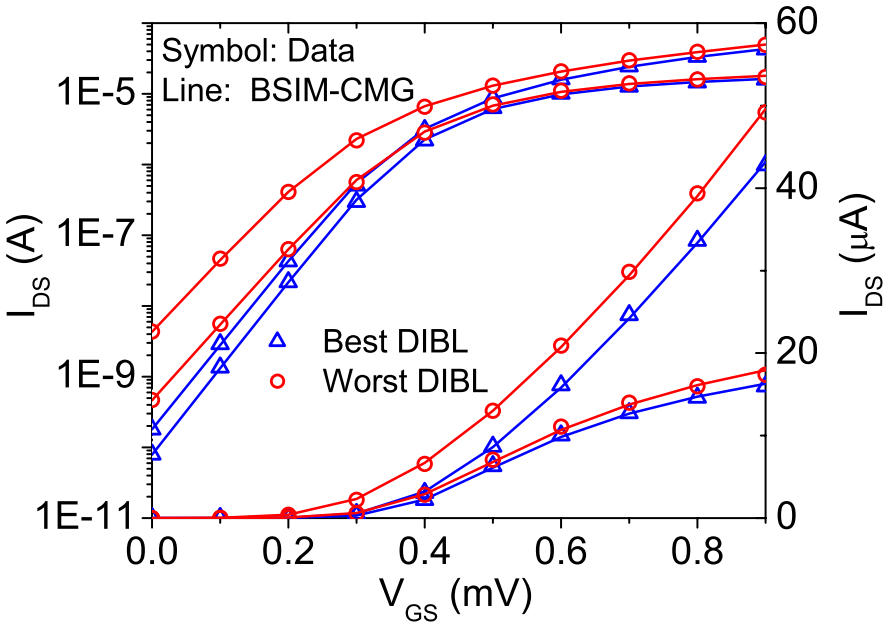




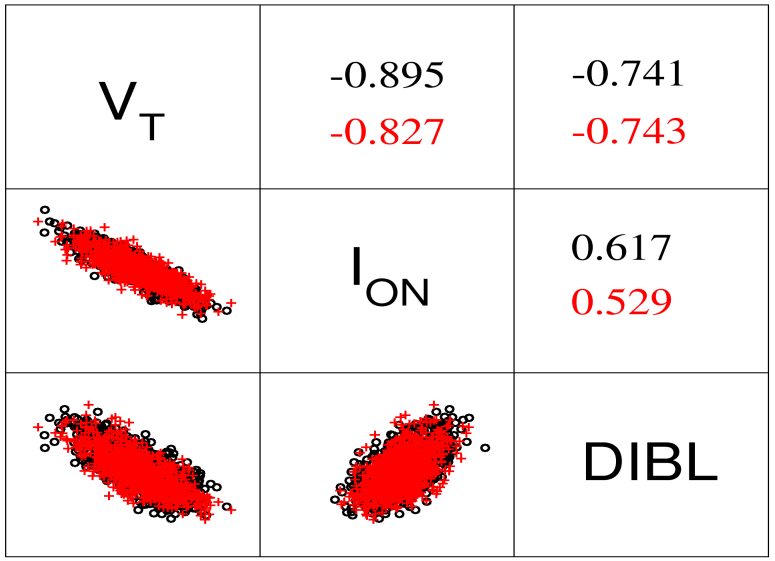


Statistical Compact Modeling

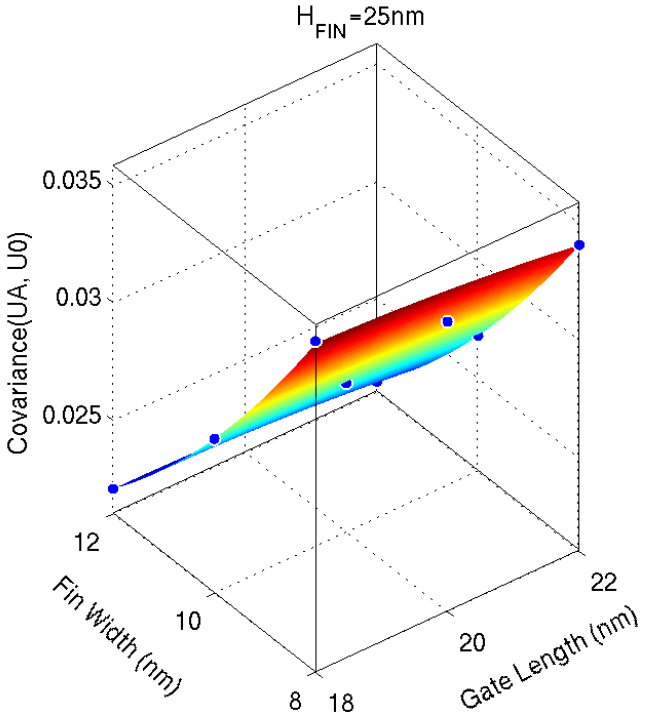


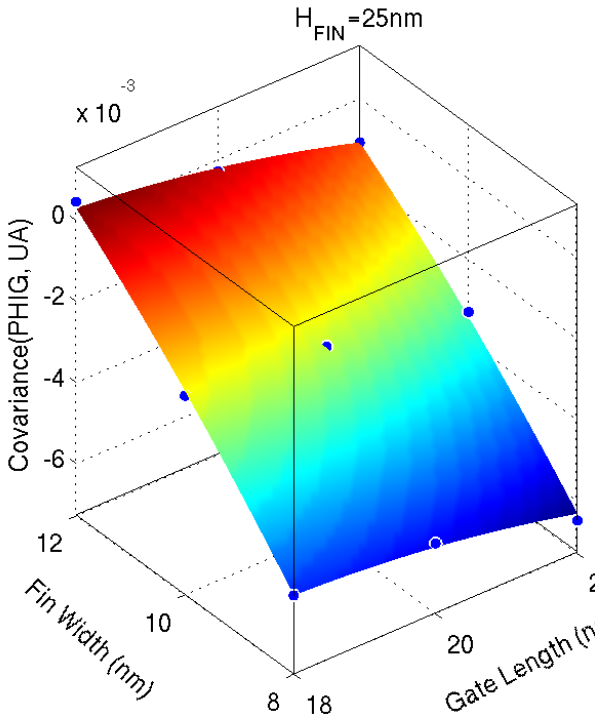


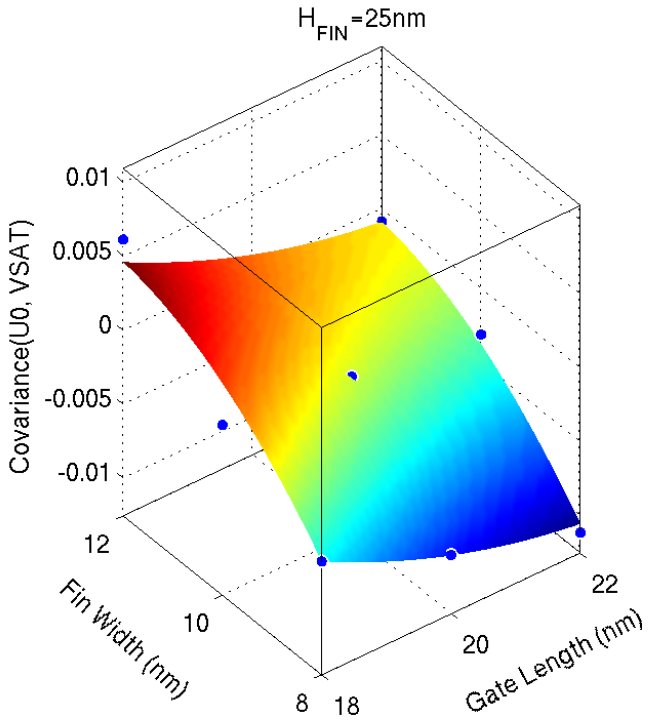
Strong correlation between statistical compact model parameter and device figure of merit demonstrates that extraction is physics based

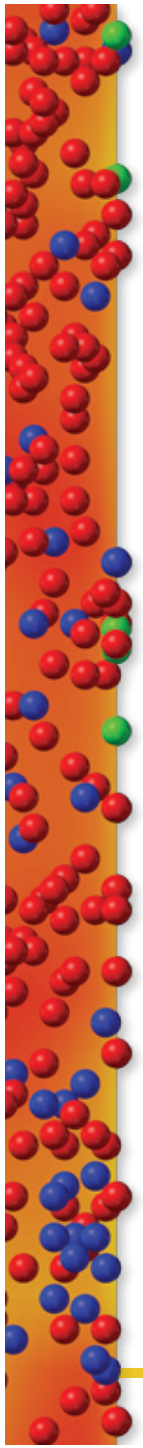


Statistical Compact Modeling – Group 2 parameter









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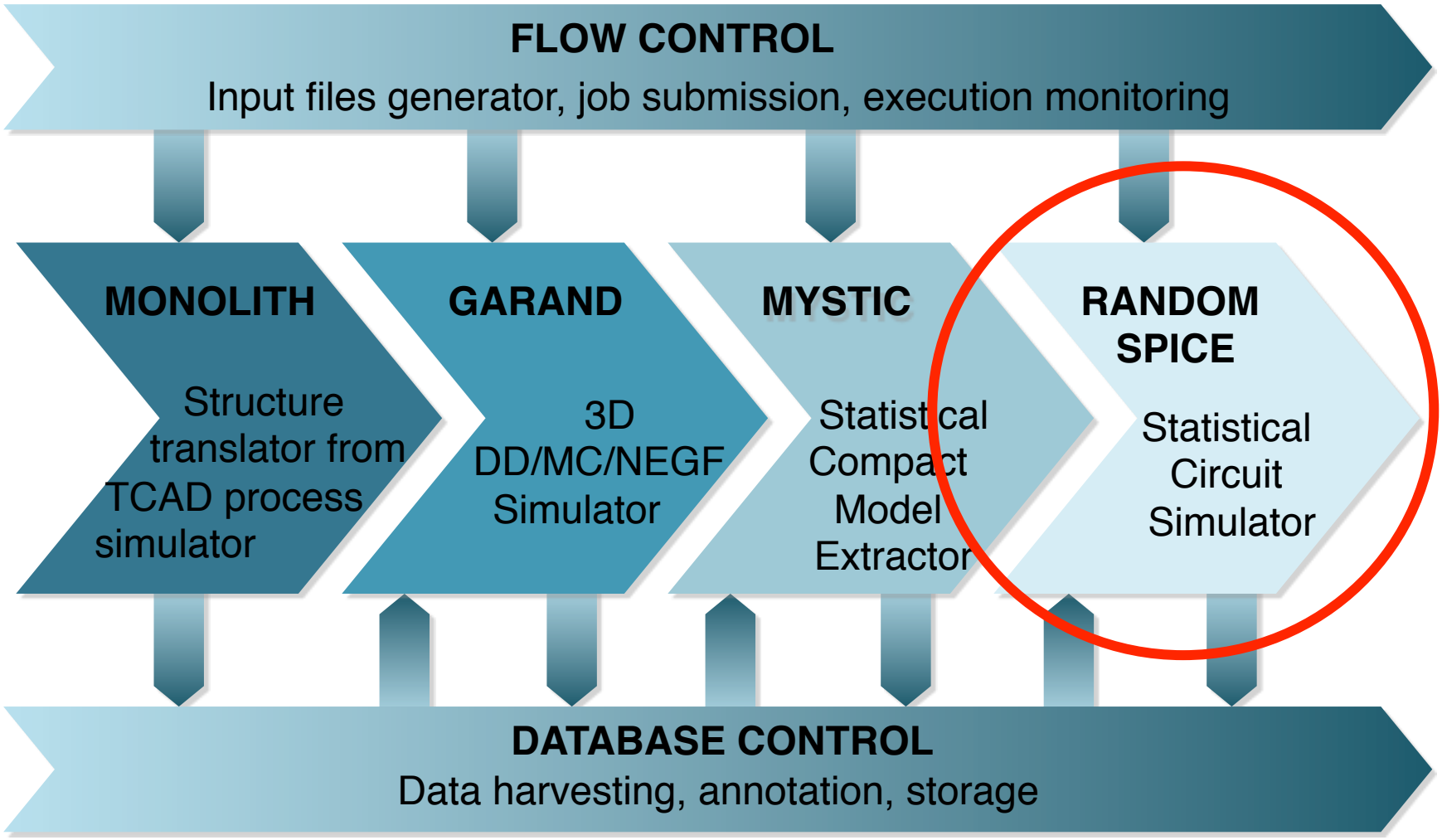
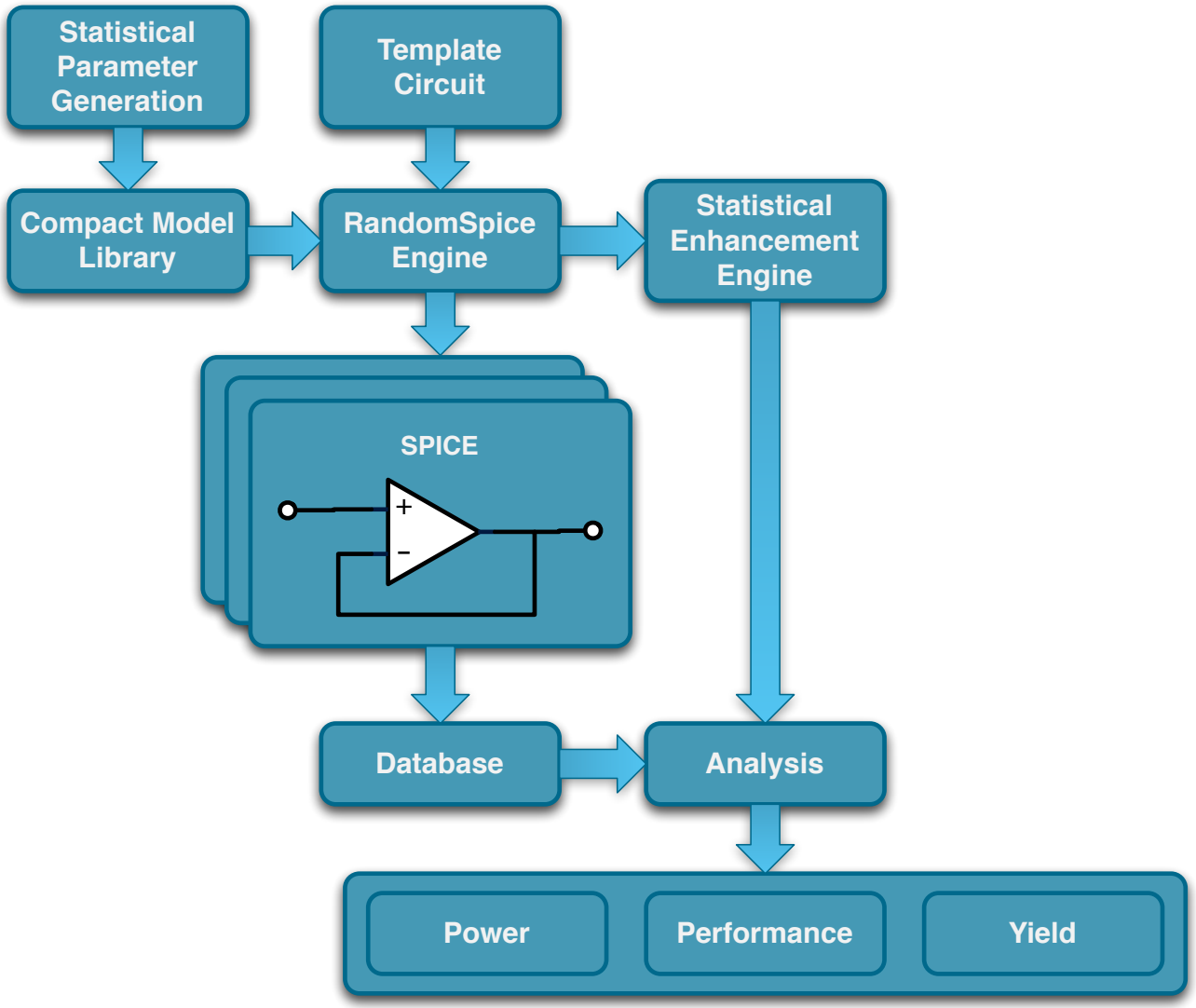
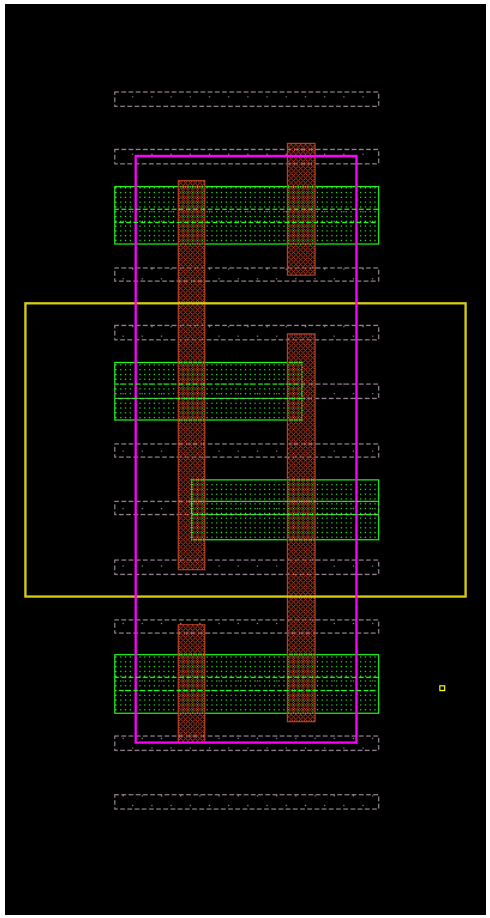


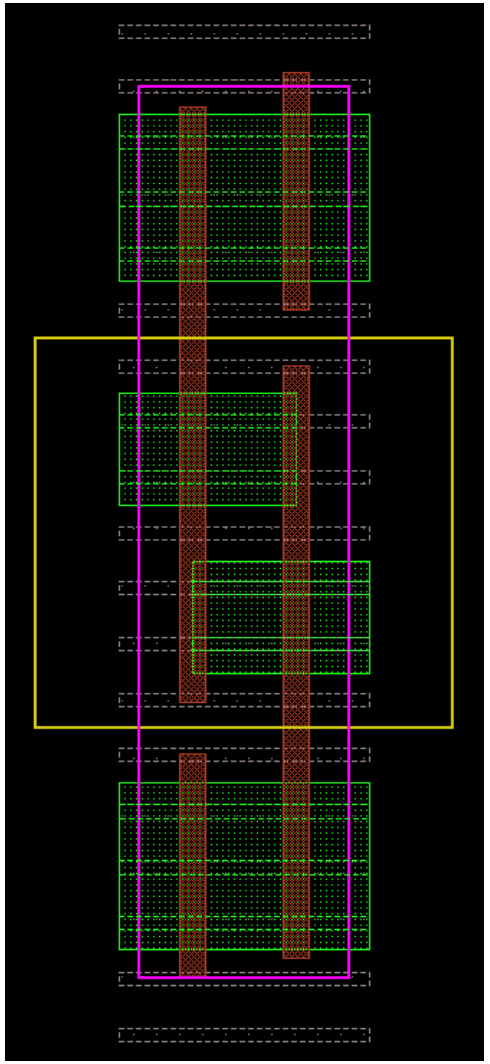
The Statistical Circuit Simulation Engine RandomSpice



FinFET based SRAM design

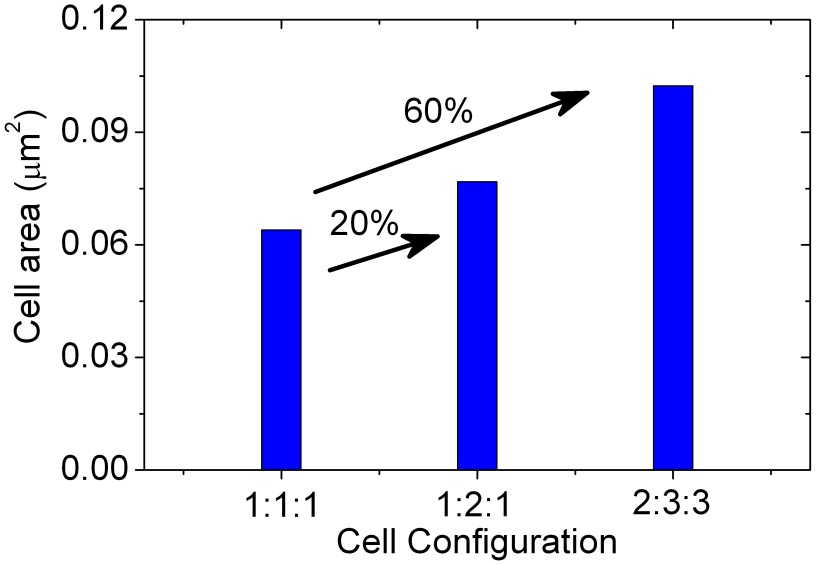


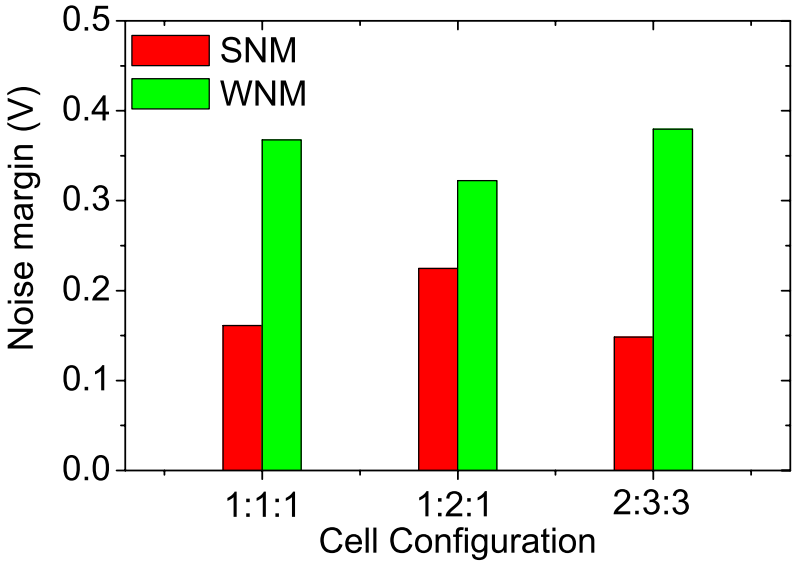
1-1-1 Cell

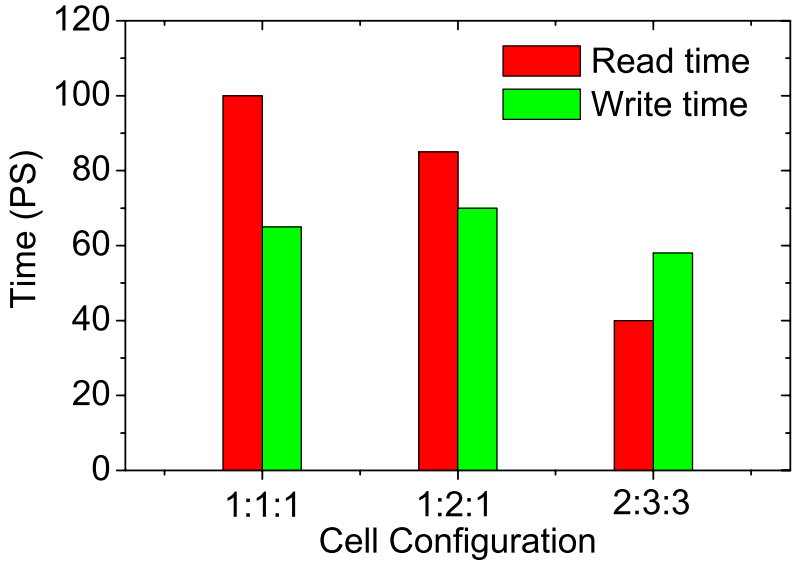


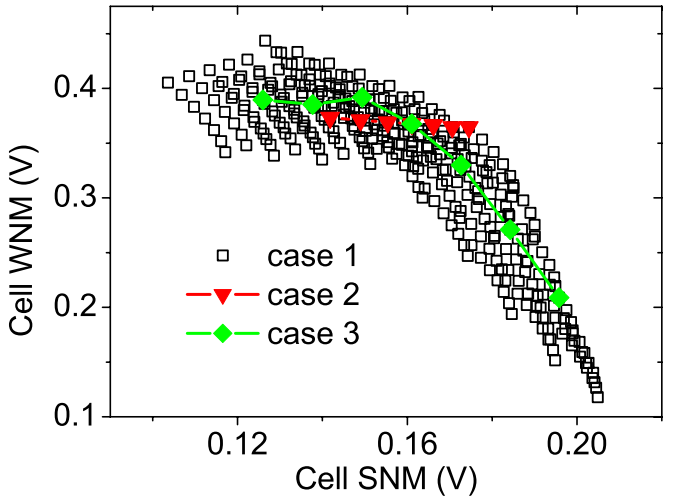
2-3-3 Cell

Cell design trade off



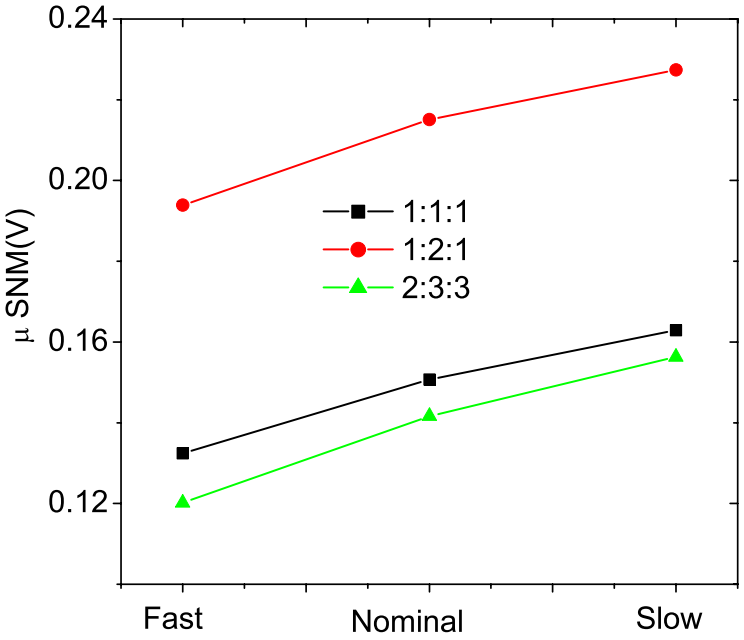


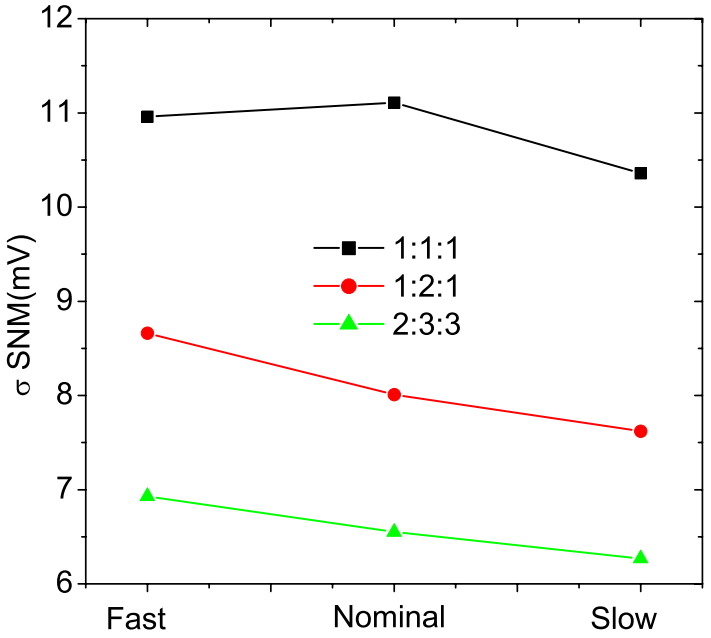


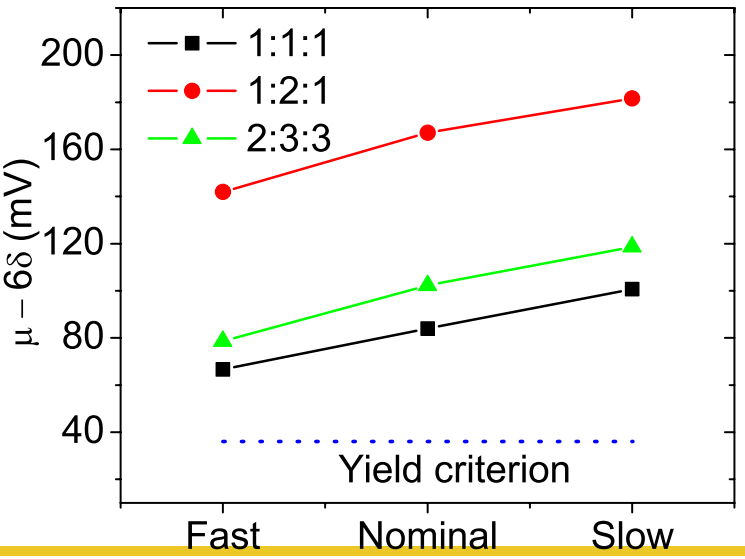


Metal Gate Work-Function Engineering

Interplay between CD and statistical variation

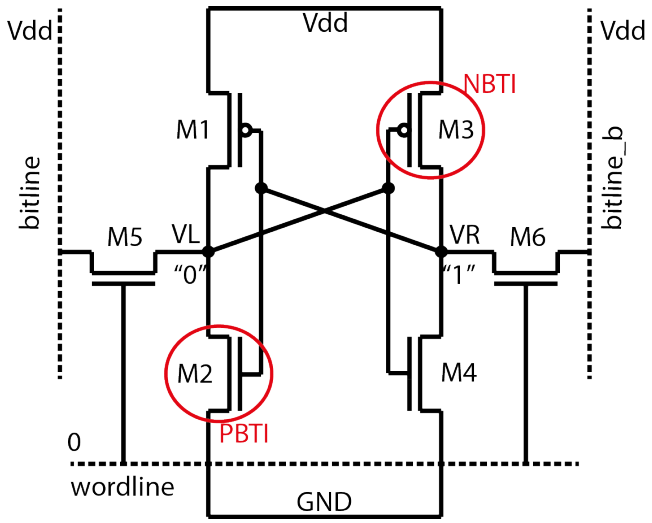


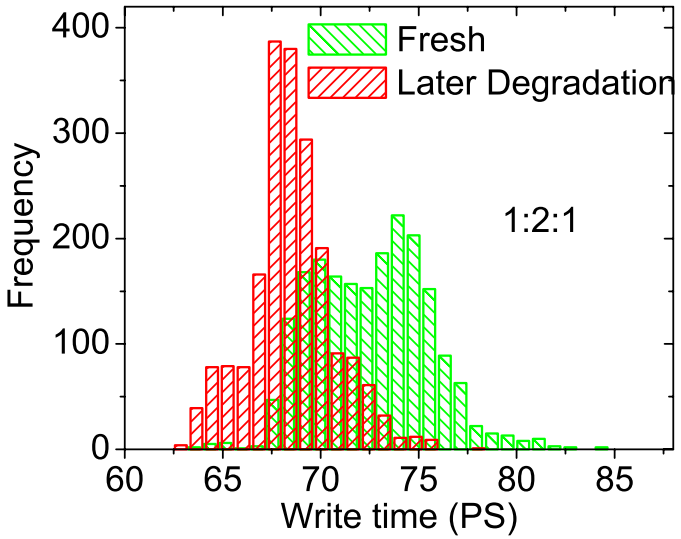


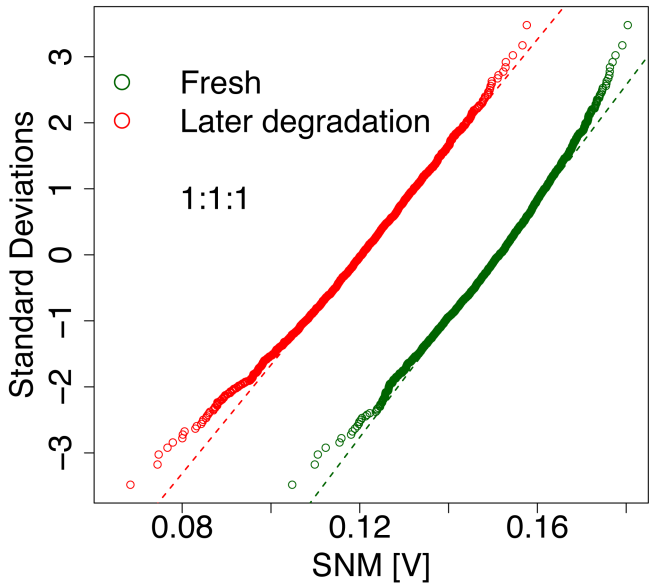


- Slow corner has the best SNM performance.
- CD variation can introduce 10% degradation on standard deviation of SNM.

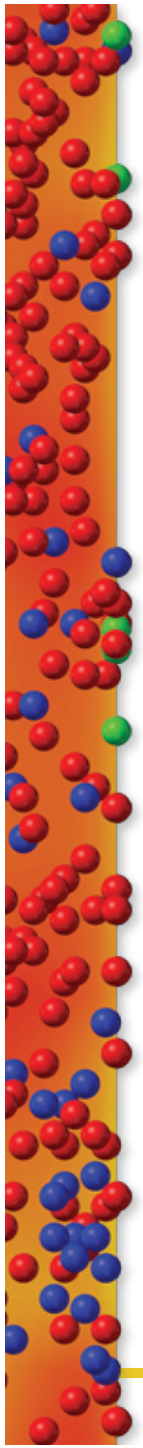
Reliability Aspect of SRAM Performance







- Under N/PBTI stress condition, SNM can be degraded by more than 25%
- However, write operation can be improved under stress condition



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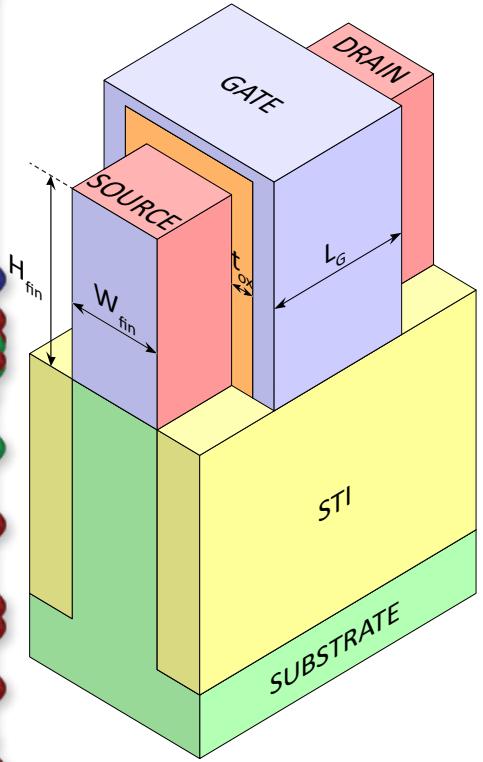
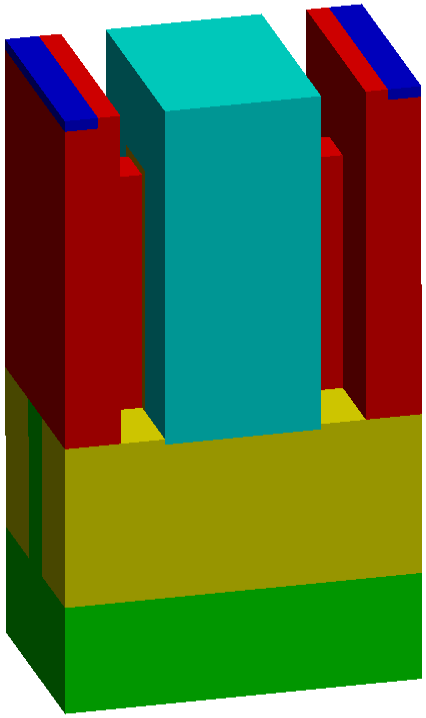
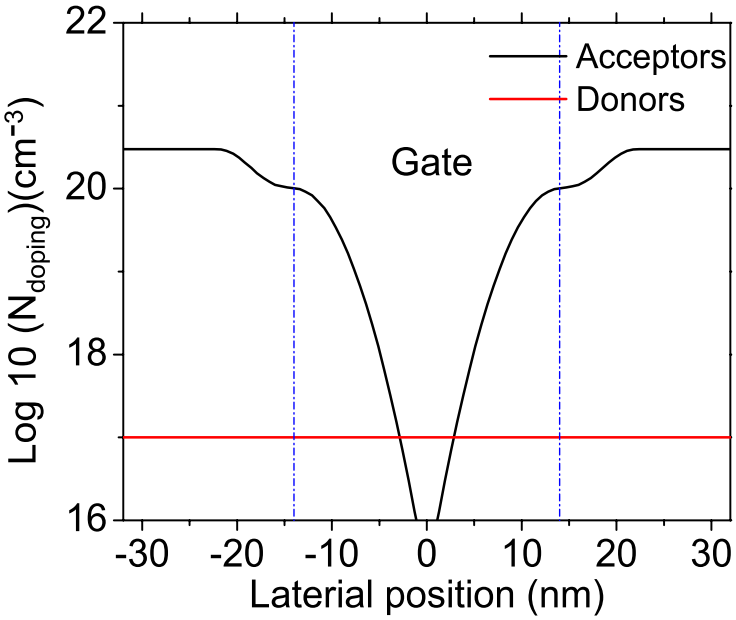
10nm FinFET options: FinFET design

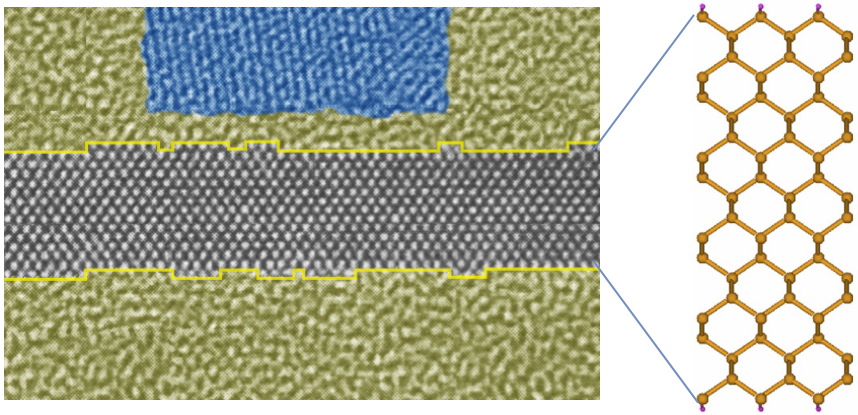


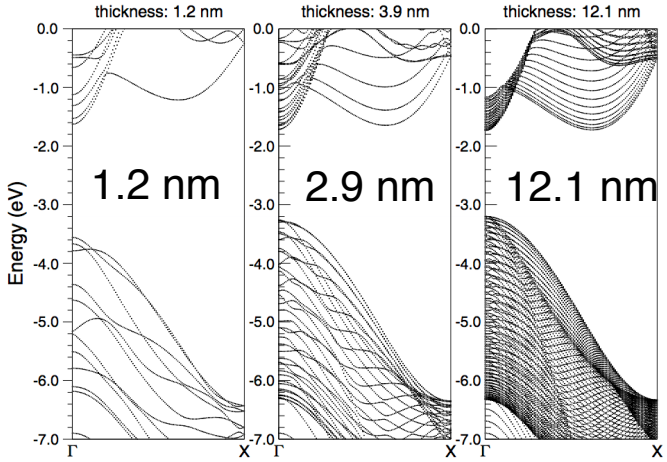


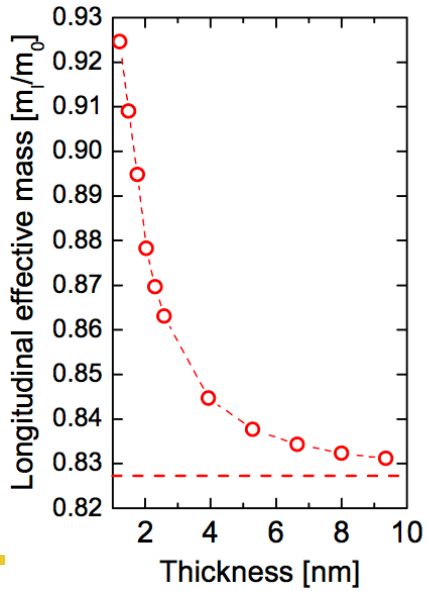


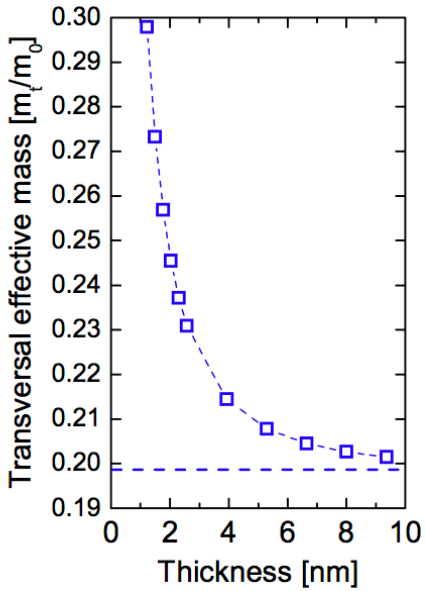
First-Principles Informed Simulations

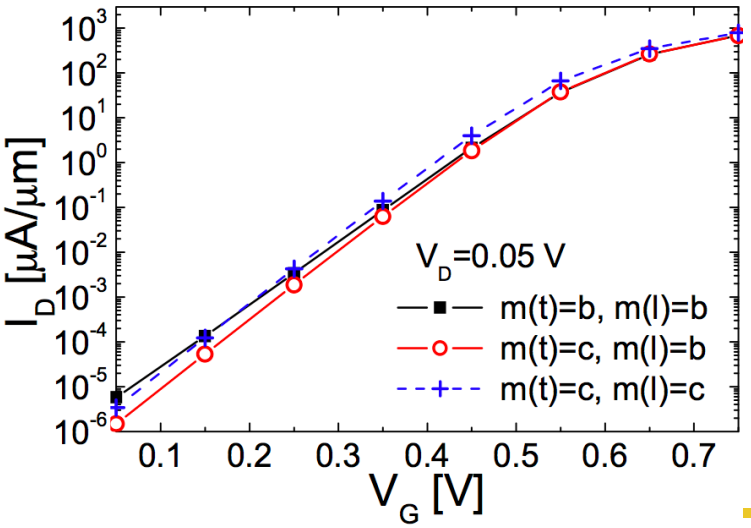
Band structure in UTB devices
(in collaboration with A. Asluger & P. Sushko, UCL)



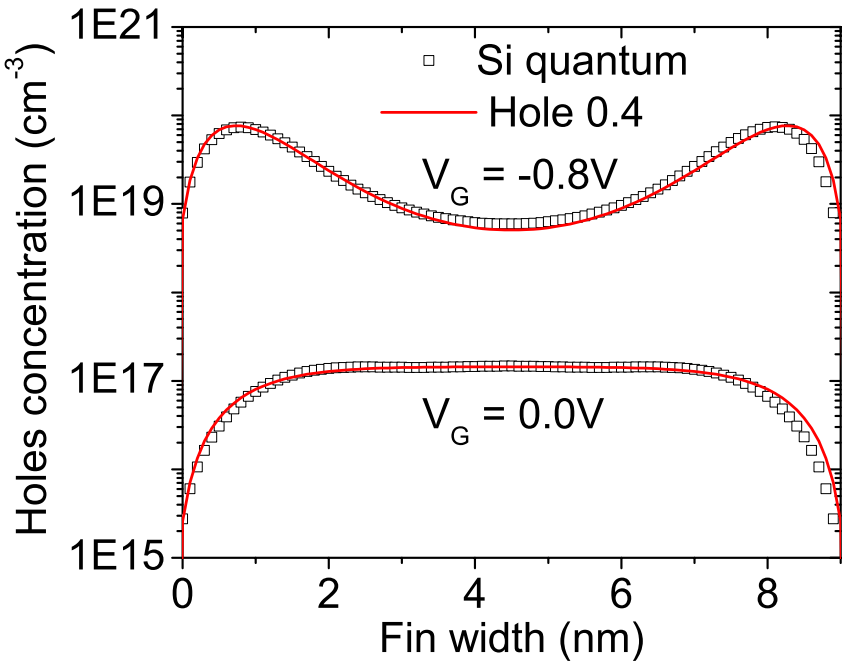


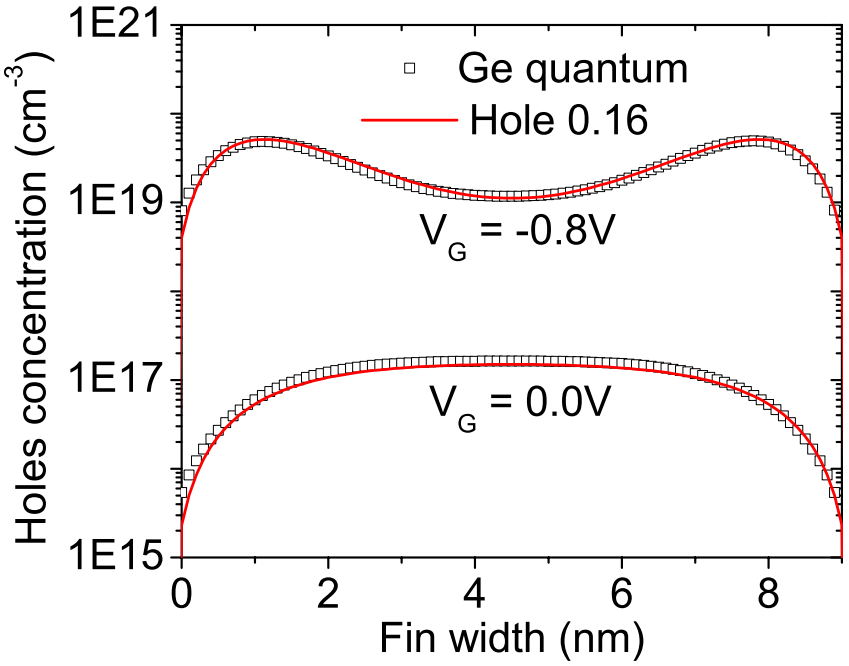




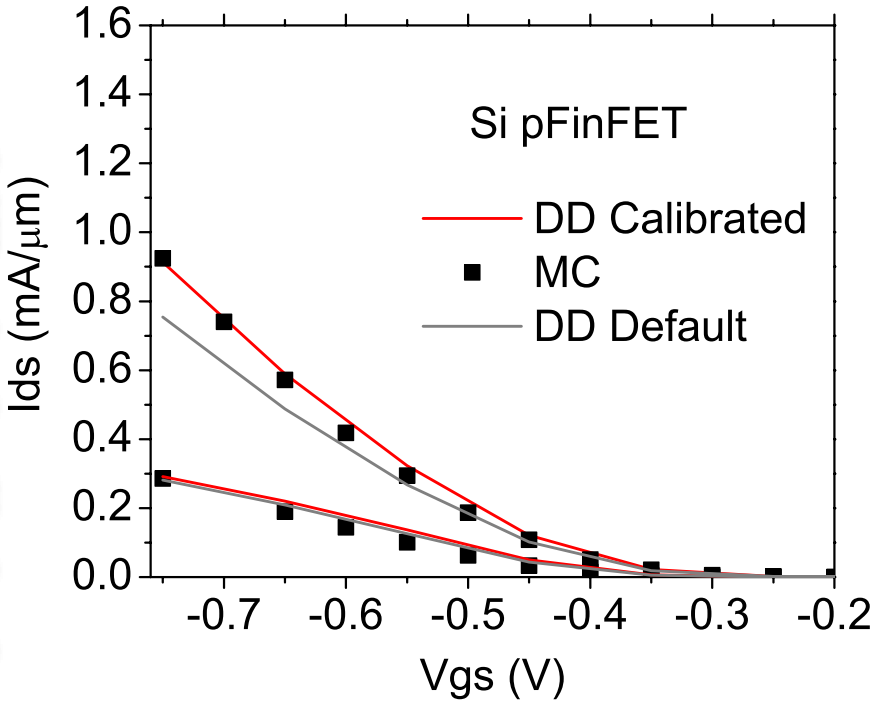


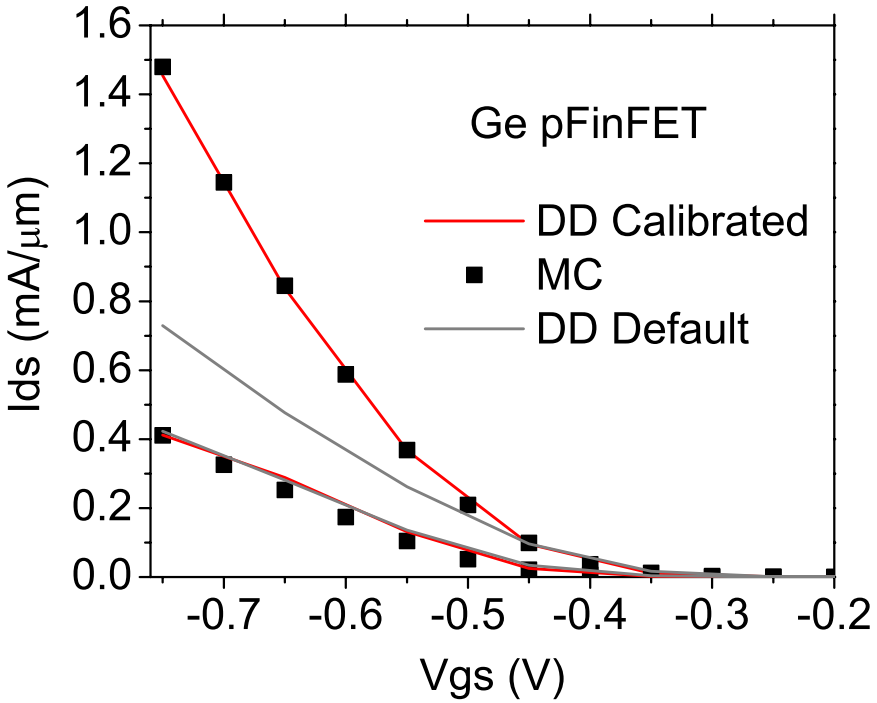
DG quantum corrections
Base on 1D Poisson-Schrodinger solver



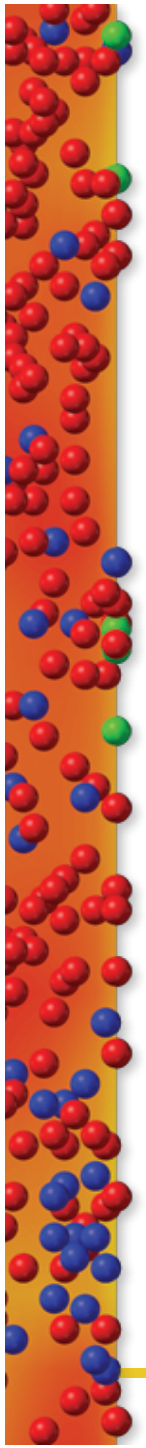


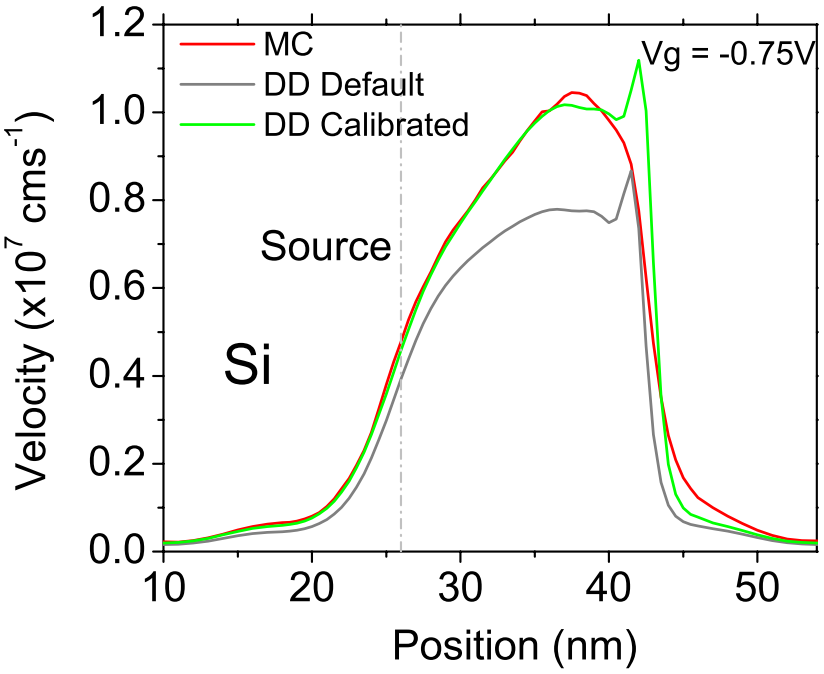
Performance based on MC simulations

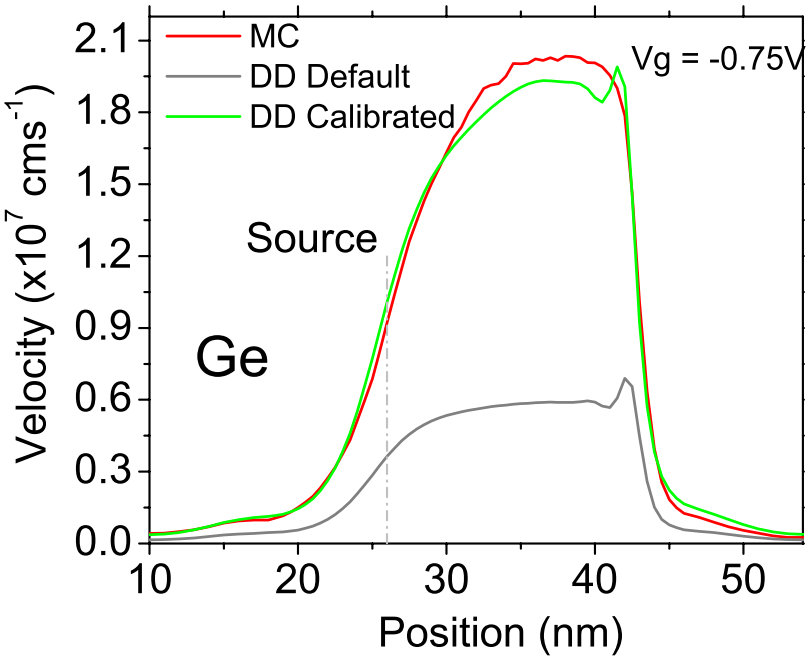




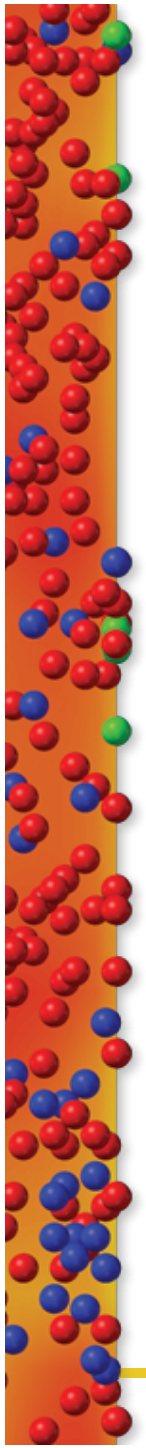
Carrier velocities

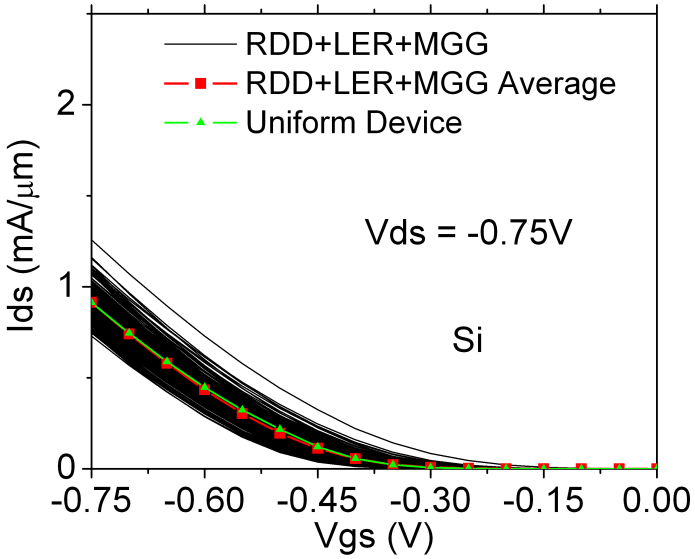


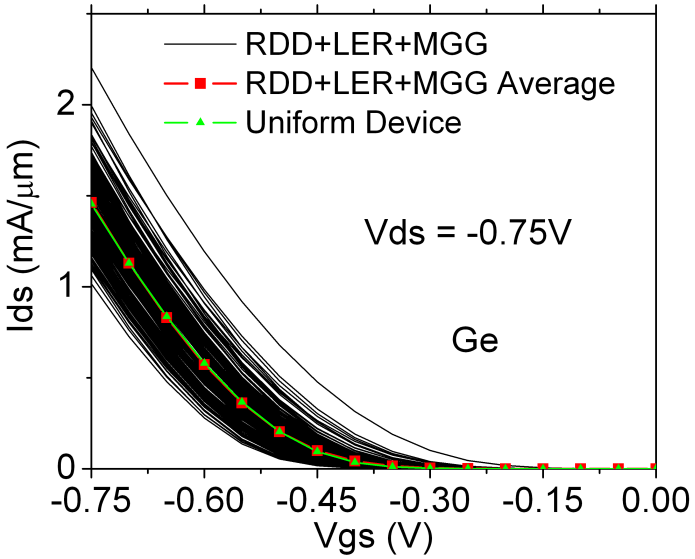


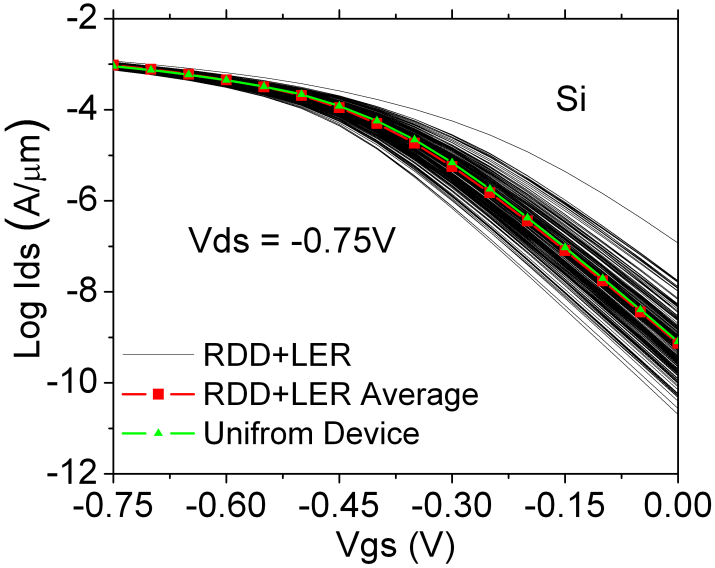


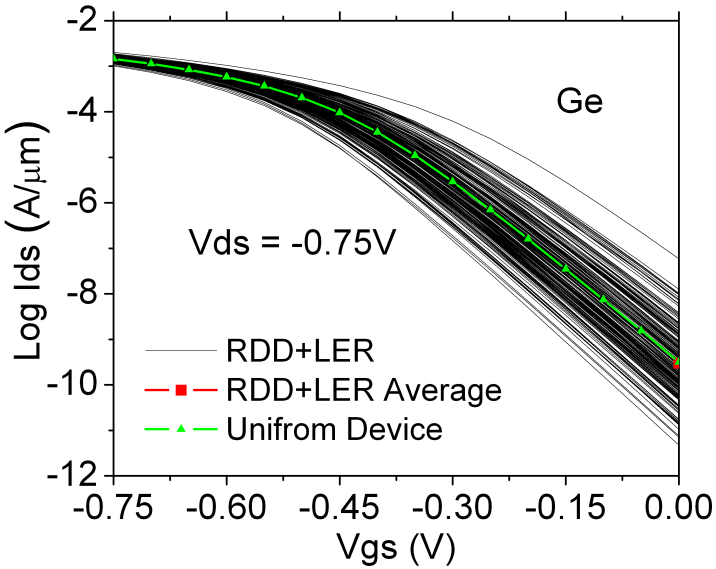
Simulation of statistical variability



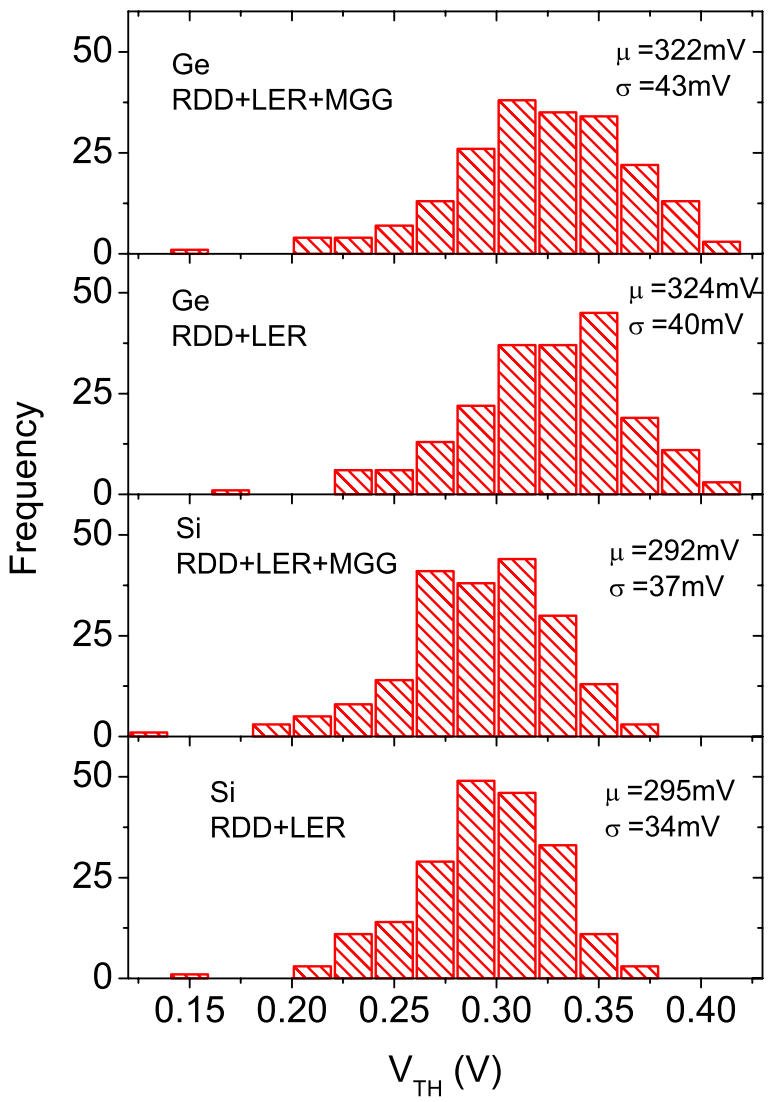


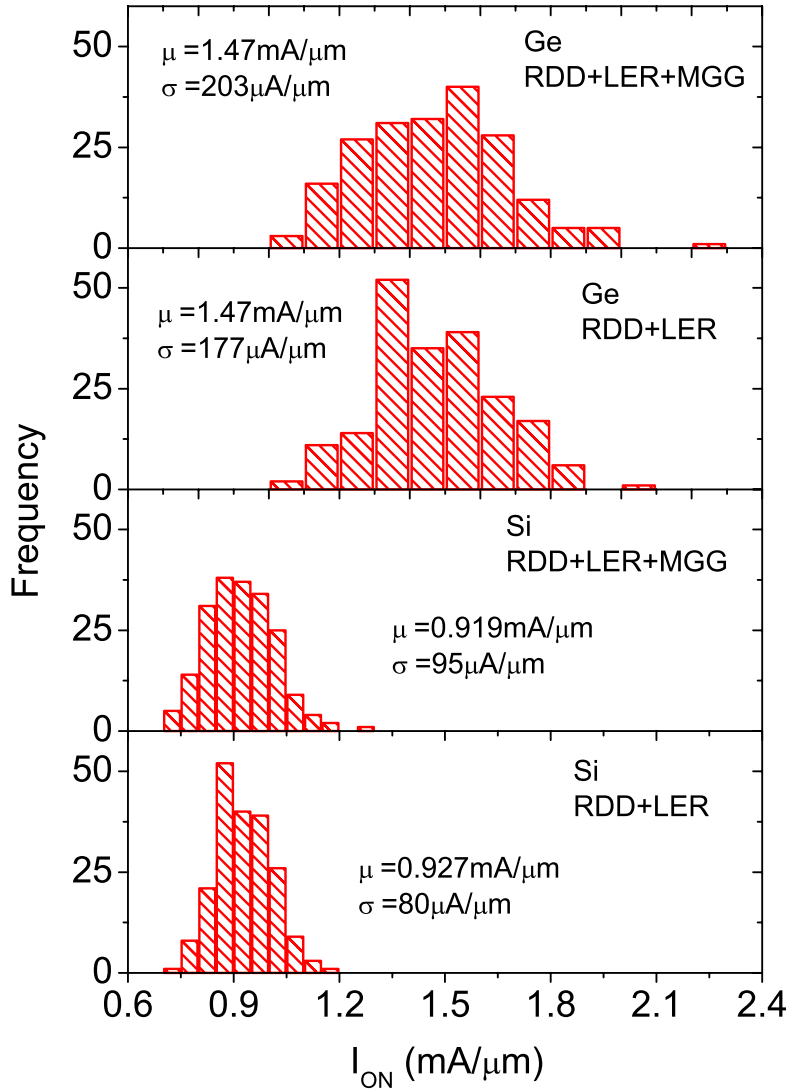




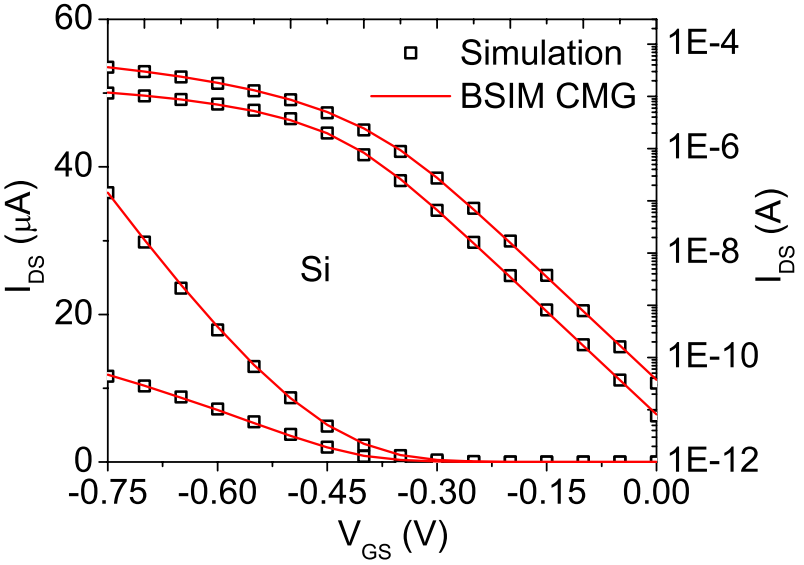


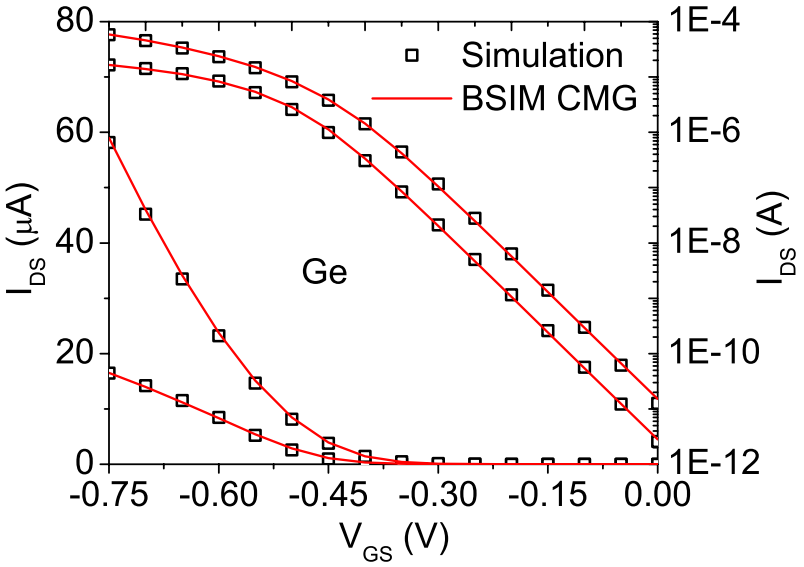
Simulation of statistical variability

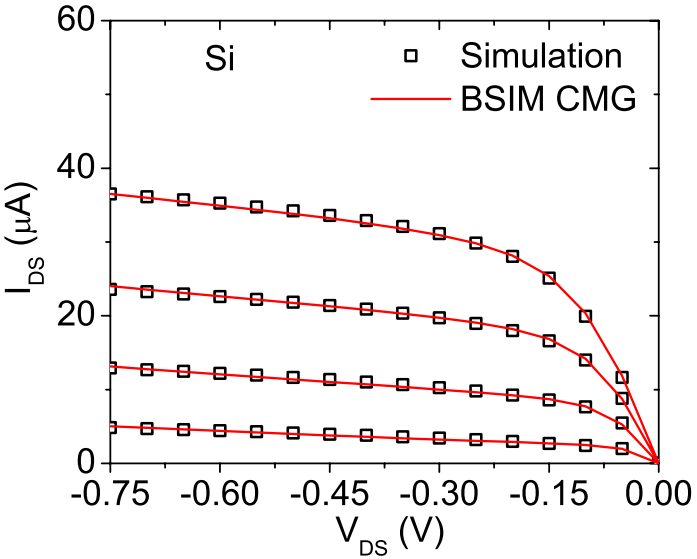


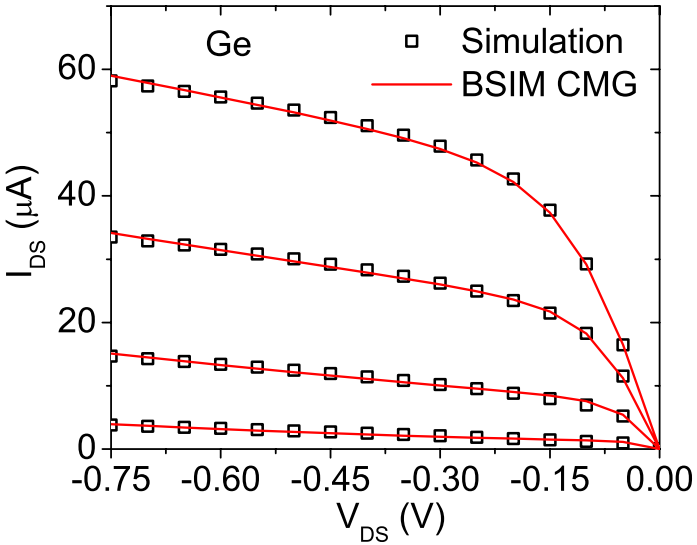


Nominal compact models

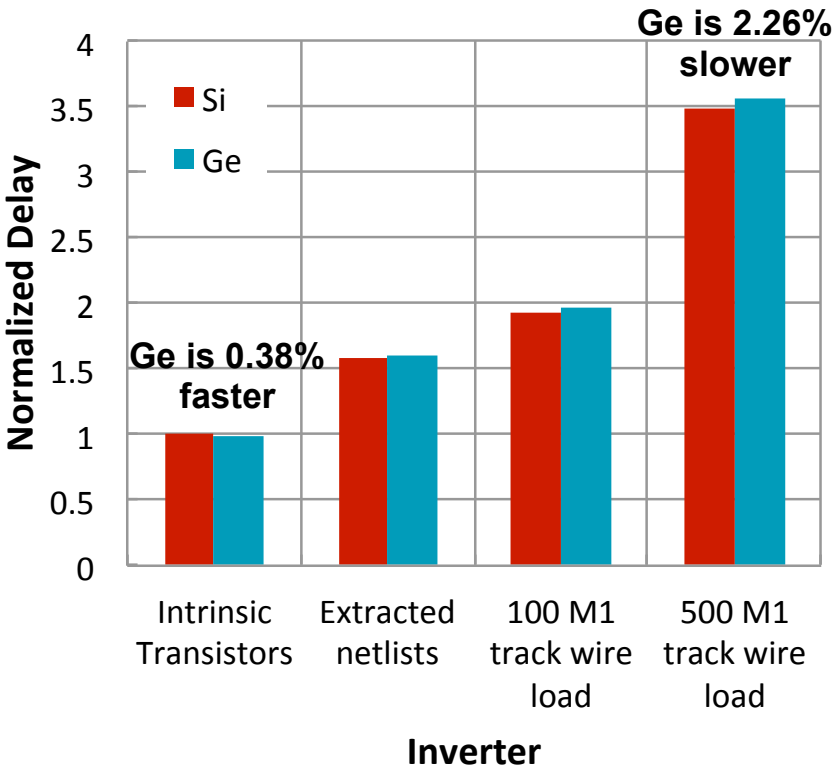


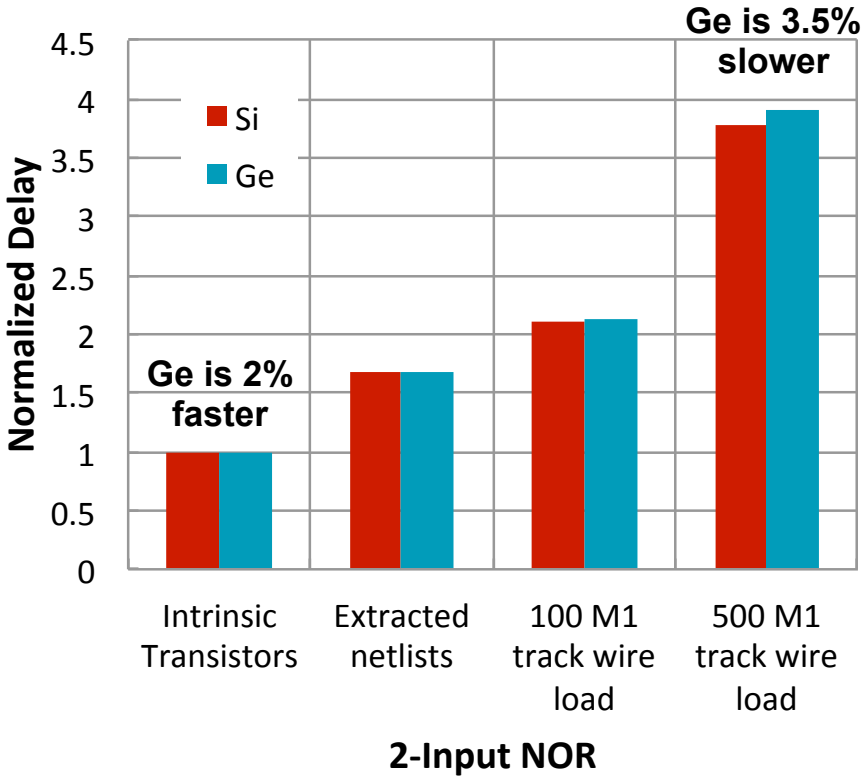






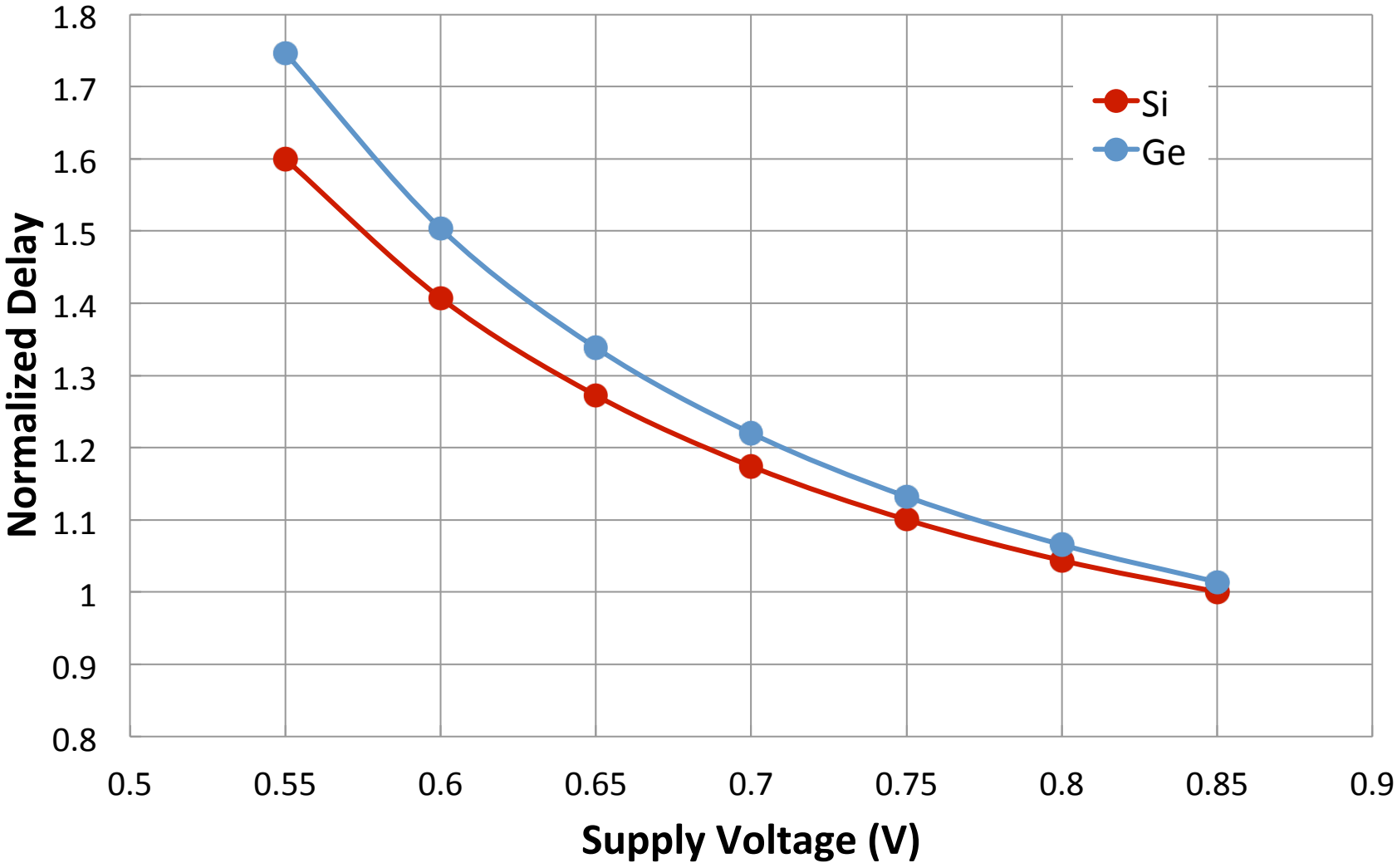
Impact of Extraction and Wire-load

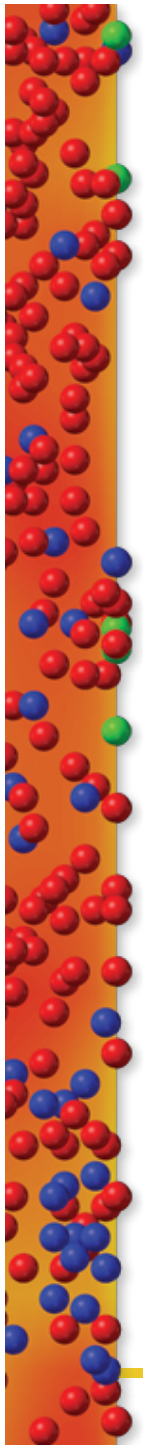




Extracted netlists generated using the ARM 10nm Predictive Technology Modeling toolset

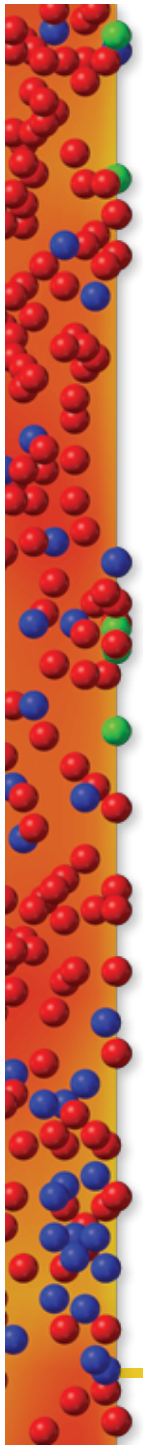
Delay vs. Supply Voltage





Conclusions

- FinFET complexity Motivates Design/Technology Co-Development.
  - 22nm Intel FinFET example
- We have studied in detail a full DTCO flow for 14nm FinFETs, showing how GSS simulation platform can help designers from process to devices up to circuit level.
- We have show an example of applicability of GSS platform for evaluating different option for future FinFETs technology generations.



Thanks for your attention!

You will find this presentation and additional material on our webpage

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